

# FPGA Based System for Human Chromosome Classification

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**Abstract**— Computer-aided systems based on artificial neural networks (ANN) are suitable for automatic chromosome classification process. However, the software based implementation of these systems running on conventional computer transforms the parallelism features of the ANN into serial operations that reduce their computation power. The hardware implementation of such system can achieve the parallelism required by ANN. This paper describes the idea of designing and implementing an FPGA (Field-programmable gate array) based system on chip (SoC) for human chromosome classification. The proposed SoC aims to realize an automatic karyotyping that helps cytogeneticist in genetic syndrome diagnosis with minimum human intervention, while reducing time, power consumption, effort and cost. The achieved part of the SoC concerns the classification subsystem based on Kohonen neural network which is the main part. The classification subsystem has been successfully implemented and tested on the Virtex5 FPGA development board. In the proposed hardware implementation of the chromosomes classifier, the total power consumption is about 0.4286W. The power consumption is noticeably reduced compared to computer based one.

**Keywords**— FPGA, Human chromosomes, Image processing, Kohonen, Neural Network, SoC.

## I. INTRODUCTION

Even today, chromosome karyotyping process and chromosome abnormalities [1] detection are performed manually in most cytogenetic laboratories. These procedures are time consuming therefore expensive [2]. The ANNs are widely employed for computer-aided system for automatic chromosome classification [2-6]. However the software based implementation of these systems running on conventional computer transforms the parallelism features of the ANN into serial operations that reduce their computation power. The hardware implementation of such system can achieve the parallelism required by the ANNs. Our goal toward this work is to design and implement a hardware system, which automates the karyotyping process and achieves the parallelism required by ANN based classifier. This paper presents an FPGA based SoC for human chromosomes classification that is being carried in our laboratory. The proposed SoC is a multistage implementation that consists of two Kohonen neural networks. The first network performs chromosomes classification according to the geometrical parameters (chromosome length (L) and centromeric index

(CI)). The second classifies the chromosomes according to the density profile (the value of each density profile (DP) is defined as the average intensity of the pixels belonging to the perpendicular line considered for each pixel along the medial axis of the chromosome). Kohonen ANN is appropriate for hardware implementation since the computation amount to apply in learning and classification phases are less than the MLP ((Multi-Layer Perceptron) or other ANNs. Herein we focus mainly on the achieved part of the SoC namely, the classification subsystem assuming the parameters extraction is already carried out in a previous work done in our laboratory [7]. The motivations behind an FPGA based SoC system for automatic chromosome classifications are mainly: Parallelism, miniaturization and power consumption reducing. FPGA based SoC for human chromosome classification is less power consuming than a computer based one that consumes hundreds of watts.

This paper is organized as follows: In section 2, we give an overview of the proposed system. The proposed architecture for hardware implementation of a Kohonen ANNs based classifier is exposed in section 3. Section 4 deals with the system prototyping results. Finally, a conclusion is given in section 5.

## II. PROPOSED SYSTEM OVERVIEW

The system scheme for automatic chromosomes analysis and classification is shown in Fig.1; it consists of four principal parts: Image acquisition, image processing, parameters extraction and classification. Each part is represented as a subsystem in the SoC architecture. The proposed design methodology begins by improving the quality of the metaphase images in order to remove the noise factors for better readability that facilitates the analysis. Then we proceed to the segmentation of the images for chromosome identification; these steps are done in the image processing subsystem. The next step is the feature extraction [8]; in this step the skeletonization is first applied to the segmented images to detect the medial axis. This latter is the approximation of the central curve of the chromosome. Three parameters, namely, chromosome length, centromeric index and density profile are extracted from the chromosome. This constitutes the features vector used later for the classification. The purpose of the classification step is to assign each chromosome to its corresponding class. In this paper we expose mainly the classification subsystem, which

is the achieved part of the SoC, the other parts are not within the scope of this paper. As shown in Fig.2 the proposed system for classification is based on multistage Kohonen ANNs. The first network recognizes chromosomes by their geometrical features (L and CI). The second network classifies the samples according to their band patterns (DP). For the two networks, Kohonen card should have a size equal to the 24 possible classes of chromosomes.

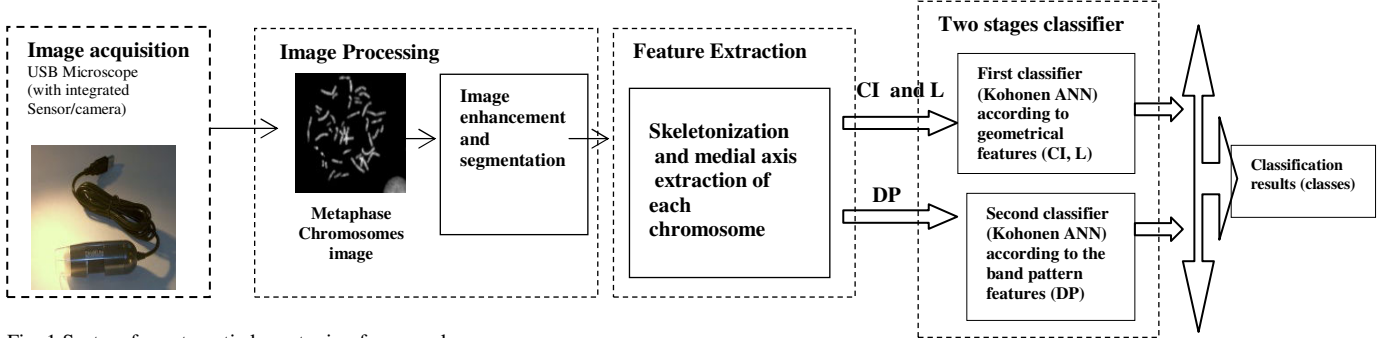


Fig. 1 System for automatic karyotyping framework

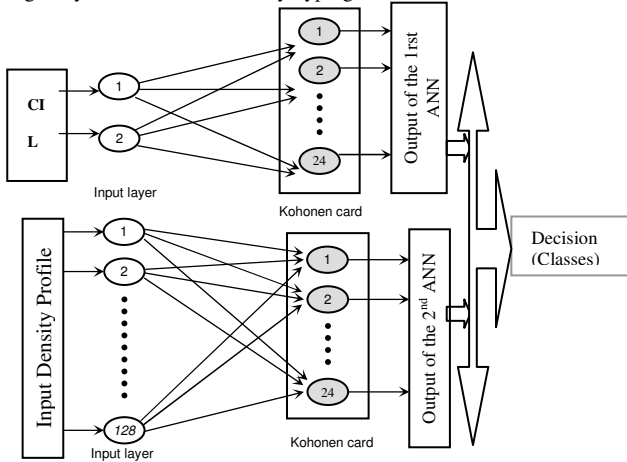


Fig. 2 Kohonen based multi-neural networks system

### III. PRESENTATION OF THE CLASSIFICATION SUBSYSTEM HARDWARE ARCHITECTURE

The proposed hardware implementation of the classifier is based on a combination of Kohonen ANNs, which includes two phases: the first phase is matching and finding the winner and the second phase is the weight updating. The proposed architecture contains a number of processing units (called neuron). In this design the inputs (or data to be processed) are chromosome length, CI and DP that constitute the features vector of the classification subsystem. These parameters are stored in the memories, MEM\_L, MEM\_CI and MEM\_DP, respectively. The features used in this work are taken from previous work done in our laboratory [7]. As classification results the indexes (classes) are ranging between 1 and 24, the sexual chromosomes X and Y are located respectively by the indexes 23 and 24. Each index will correspond to a class and thus to a unit (neuron) in the Kohonen network.

#### A. The learning phase

The learning phase starts with the weight vectors initialization, then the distance of each input vector to all weight vectors is calculated in order to determine the winning neuron, also called best matching unit (BMU); which is the one with the smallest distance.

In the proposed architecture we have used the Manhattan metric for distance computation and the winning neuron detection instead of the Euclidean distance; in order to simplify the computation and reduce the area utilization. Fig.3 represents the block diagram of the learning phase architecture, which consists of three principal components namely, chromosomal parameters memorization block, distance computation & winning neuron determination block and weight update block.

#### B. Classification phase

In the classification phase, the indexes corresponding to chromosome pairs of the karyotype are the results given in outputs. The weights used in this part are determined by the weight update block in the learning phase. Fig.4 represents the block diagram of the classification phase architecture; the chromosome classification results are displayed on the FPGA platform LCD screen after physical implementation. These results confirm the validity of our classifier based on Kohonen neural hardware implementation.

### IV. SYSTEM PROTOTYPING

#### A. Synthesis results

The achieved subsystem has been prototyped using the Xilinx development platform ML501-Virtex5, The operating frequency is 48 MHz. The development tool used for the design and implementation is the ISE 13.1 tool [9]. Table 1 summarizes the synthesis results; the achieved part of the SoC uses 16 % of Slice registers and 77% of Slice LUTs. It is noticeable that the Slice LUTs are the most used resources, the use of other resources remain low. The tool used to estimate the power consumption is Xilinx XPower Analyzer. The total power consumption is about 0.429 W, with 0.347W as static power and 0.082W as dynamic power.

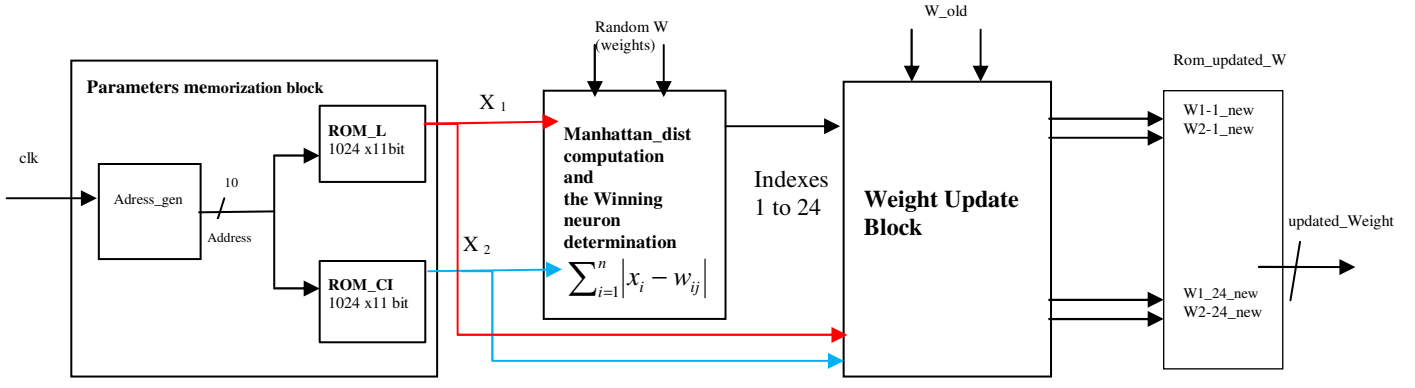


Fig.3. Learning phase architecture block

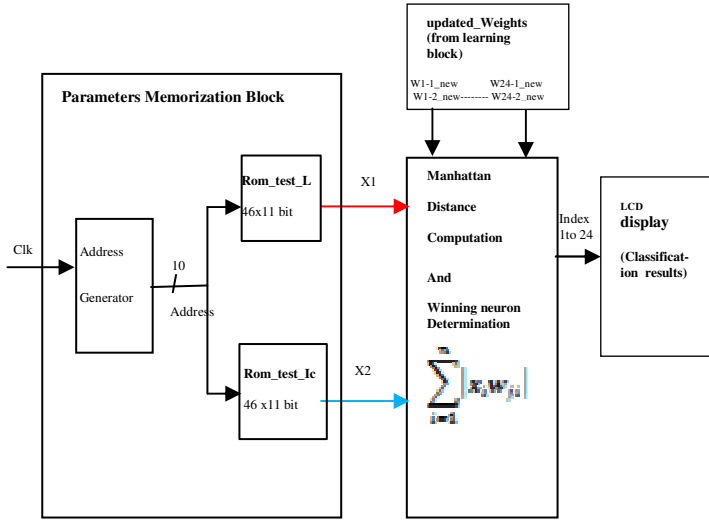


Fig.4. Classification phase architecture block diagram

TABLE I  
SYNTHESIS RESULTS. TARGET DEVICE XC5VLX50-1FF676

Slice Logic resources	Used Slice Logic	Available Slice Logic	% Occupied resources
Number of Slice registers	4883	28800	16%
Number of Slice LUTs	22457	28800	77%
Number of bonded IOBs	6	440	1%

### B. Recognition rate

For each chromosome, 130 (128 DP + CI + L) features have been used in the compound classifier. The chromosomes classifier was tested on a database which contains 11 metaphase images (chromosomes images taken at the third phase of cell division). The database includes normal and abnormal numerical aberration cases that include either missing chromosome (monosomy) or extra chromosome (trisomy). Trisomy can affect some pairs of autosomes (13, 18 and 21) or sex chromosomes. Fig.5. represents the recognition rate according to the weighted coefficients of band pattern and morphological parameters. Several

combinations of both geometrical and band pattern (DP) features were used to evaluate the recognition rate. The results show that for several combinations (DP, CI+L, DP+CI+L) the morphological features (L, CI) give better recognition rate than density profile when used separately, but we notice that the combination of the features including band pattern (DP) and geometrical features gives a maximum recognition rate of our architecture, which is about 65.5 %.

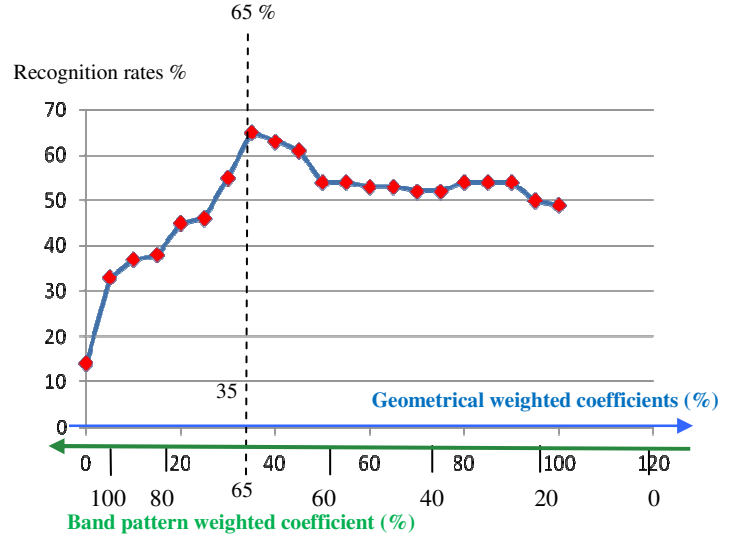


Fig.5 Recognition rate results according to weighted coefficients (%) of band pattern and morphological parameters

### V. CONCLUSION

Promising results have been achieved regarding the realized part of the SoC that concerns the classification subsystem based on the hardware implementation of a combination of Kohonen ANNs. This subsystem is the main part of the SoC for an FPGA based automatic karyotyping. Morphological and density profile features have been used for classification. The combination of the features including band pattern and geometrical features gives a maximum recognition rate of our architecture, which is about 65.5 %. The obtained recognition rate is similar to the classifier (software implementation) exposed in a previous work [7] done in our laboratory (the same chromosomes images database was used). Compared to the state-of-art methods related to software based chromosomes classifiers, the obtained result is quite competitive and it is still acceptable. The chromosomes

classification results are displayed on the FPGA platform LCD screen after physical implementation. The synthesis results show that the classifier architecture can be mapped into the ML501-Virtex5 FPGA platform; it occupies 77 % of logic resources. The extension of the realized part of the proposed system by the creation of additional subsystem namely; image acquisition, image processing, parameters extraction are topics of future works; in order to build a portable system which constitutes an automatic karyotyping. It is noteworthy to precise that the point of the exposed work is not to compete with commercial systems in clinical laboratories; but rather to propose a contribution in this area of research that is still an open issue. We suppose that a hardware system will be suitable for use in clinical laboratories.

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