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Study of the UPQC facing voltage and current disturbances

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Abstract— Unified Power Quality Conditioner (UPQC) is one of the custom power devices that are used as an effective solution. The series active filter (SAF) which is used to compensate voltage disturbances and the parallel active filter (PAF) which is used to compensate current disturbances and reactive power. The UPQC is the combination of both SAF and PAF.

Keywords— UPQC, Active filter, harmonic, THD, MLI

I. INTRODUCTION

UNIFIED POWER-QUALITY (PQ) conditioner (UPQC) systems were widely studied by many researchers as an eventual method to improve the PQ in electrical distribution systems [1][2]. The aim of a UPQC is to eliminate the disturbances that affect the performance of the critical load in power systems. The UPQC, therefore, is expected to be one of the most powerful solutions to large-capacity loads sensitive to supply-voltage-imbalance distortions [3]. The UPQC, which has two inverters that share one dc link, can compensate the voltage sag and swell and the harmonic current and voltage, and it can control the power flow and voltage stability. Moreover, the UPQC with the combination of a series active power filter (APF) and a shunt APF can also compensate the voltage interruption if it has some energy storage or battery in the dc link [4].

The shunt APF is usually connected across the loads to compensate for all current-related problems, such as the reactive power compensation, power factor improvement, current harmonic compensation, neutral current compensation, dc-link voltage regulation, and load unbalance compensation, whereas the series APF is connected in series with a line through a series transformer (ST). It acts as a controlled voltage source and can compensate all voltage-related problems, such as voltage harmonics, voltage sag, voltage swell, flicker, etc. [5], [6].

II. UPQC—STATE OF THE ART

There are two important types of APF, namely, shunt APF and series APF [7] [8]. The shunt APF is the most promising to tackle the current-related problems, whereas, the series APF is the most suitable to overcome the voltage-related problems. Since the modern distribution system demands a better quality of voltage being supplied and current drawn, installation of these APFs has great scope in actual practical implementation. However, installing two separate devices to compensate voltage- and current-related power quality problems, independently, may not be a cost effective solution. Moran [9] described a system configuration in which both series and shunt APFs were connected back to back with a common dc reactor. The topology was addressed as line voltage regulator/conditioner. The back-to-back inverter system configuration truly came into attention when Fujita and Akagi [10] proved the practical application of this topology with 20 kVA experimental results. They named this device as unified power quality conditioner (UPQC), and since then the name UPQC has been popularly used by majority of the researchers [11] [12] [13] [14] [15], The back-to-back inverter topology has been also addressed as series–parallel converter [16].

In construction, a UPQC is similar to a unified power flow controller (UPFC) [5]. Both UPQC and UPFC employ two voltage source inverters (VSIs) that are connected to a common dc energy storage element. A UPFC is employed in power transmission system whereas UPQC is employed in a power distribution system, to perform the shunt and series compensation simultaneously. However,

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a UPFC only needs to provide balance shunt and/or series compensation, since a power transmission system generally operates under a balanced and distortion free environment. On the other hand, a power distribution system may contain dc components, distortion, and unbalance both in voltages and currents. Therefore, a UPQC should operate under this environment while performing shunt and/or series compensation.

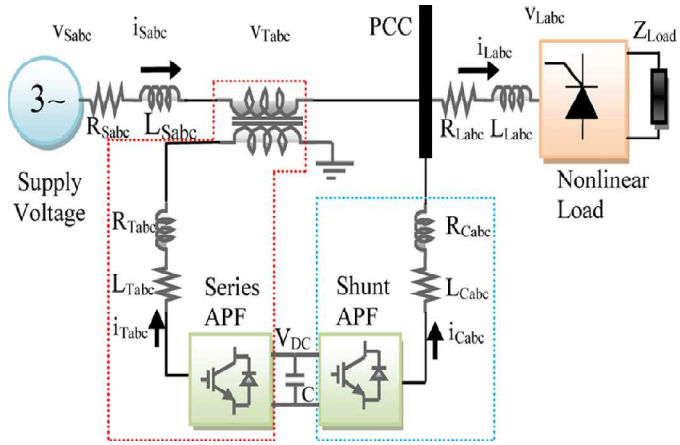

Fig. 1. Basic system configuration of UPQC.

The main purpose of a UPQC is to compensate for supply voltage power quality issues, such as, sags, swells, unbalance, flicker, harmonics, and for load current power quality problems, such as, harmonics, unbalance, reactive current, and neutral current. Fig. 1 shows a single-line representation of the UPQC system configuration. The key components of this system are as follows.

1) Two inverters—one connected across the load which acts as a shunt APF and other connected in series with the line as that of series APF.

2) Shunt coupling inductor LSh is used to interface the shunt inverter to the network. It also helps in smoothing the current wave shape. Sometimes an isolation transformer is utilized to electrically isolate the inverter from the network.

3) A common dc link that can be formed by using a capacitor or an inductor. In Fig. 1, the dc link is realized using a capacitor which interconnects the two inverters and also maintains a constant self-supporting dc bus voltage across it.

4) An LC filter that serves as a passive low-pass filter (LPF) and helps to eliminate high-frequency switching ripples on generated inverter output voltage.

5) Series injection transformer that is used to connect the series inverter in the network. A suitable turn ratio is often considered to reduce the current or voltage rating of the series inverter.

III. IDENTIFICATION METHODE

The PLL method is a perturbation identification method used to extract the phase of the direct fundamental component of voltage (δd). Moreover, this method makes it possible to calculate the amplitude of the fundamental fundamental component Vd using a low-pass filter. The voltage applied in the identification method is a three-phase voltage (Vd123) supplied by a PLL-based system. The voltage of the network must be sound (sinusoidal and balanced), otherwise the instantaneous power method is not applicable. Since the mains voltage is often disturbed and / or distorted.

The principle of PLL is based on the use of an RST regulator, guaranteeing a good level of reliability and a fast response . Its operation is based on the transformation of Park in the reference d, q. fig (3)

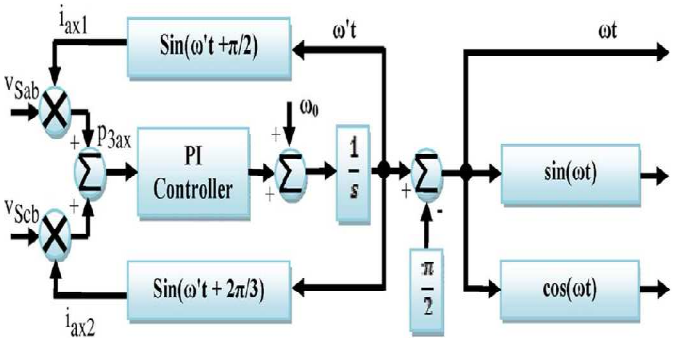

Fig. 3 Modified PLL circuit block diagram.

A. *The voltage inverter*

A three-phase inverter with a voltage structure. It consists of three arms with reversible switches, controlled by closing and opening, made from a transistor (GTO or IGBT) and a diode in antiparallel. (4). [3]

The voltage inverter interfaces between two types of source:

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An alternate rated source which must never be in open circuit, the current flow must always find a free path from where the antiparallel of diodes with the switches

A voltage source at the terminals of the inverter must never be short-circuited, so the two switches on the same arm must have two additional controls.

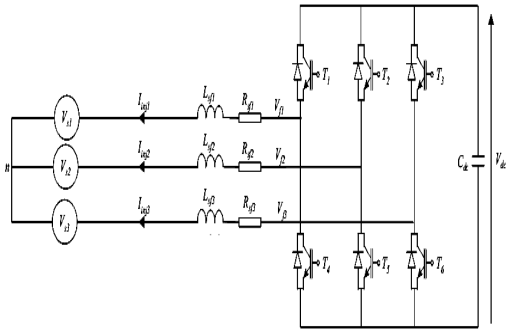

Fig. 4 the voltage inverter

The voltage inverter controlled by the MLI control, the purpose of which is to enable the best reproduction of the reference perturbed currents, through the control commands applied to the power switch drivers.

The output voltage of the inverter is:V_{sf} =K.V_m with K=$\frac{Vdc}{2.Vp}$

B. MLI control

The MLI command is generally the most complex in the control families of the inverter since it is often based on two control loops:

An external current loop

An internal tension loop.

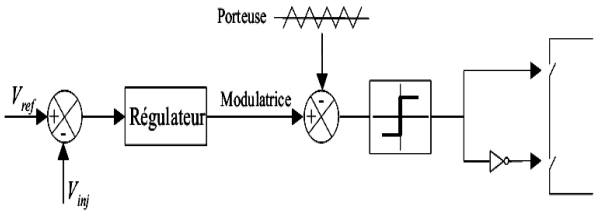

Fig. 5 The control loop of the inverter by MLI three-phase voltage

The technique of this control solves the problem of controlling the switching frequency by operating with a fixed frequency that is easy to filter downstream of the inverter.

The intersected MLI technique is undoubtedly the simplest and best known technique of MLI. It first uses a regulator which generates the reference voltage to the inverter (modulator) from the difference between the measured current and its reference. The latter is then compared with an auxiliary (carrier) signal which may be sawtooth or triangular with a fixed frequency fp that is sufficiently high with respect to the maximum reference frequency. The comparator output provides the control command of the switches (points of intersection of the two signals).

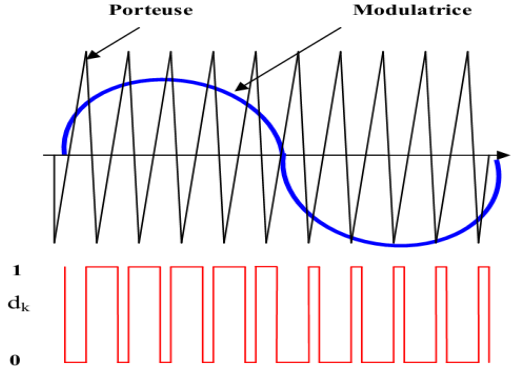

Fig. 6 The principle of operation of the voltage inverter by MLI

C. The regulation loop

The corrector PI is a corrector of the type one corrector of the proportional type Kc and the other of the integrator type Ki / S. It is often modeled by its following transfer function

$$G(s) = K_c + \frac{K_i}{S}$$

The choice of the parameter Kc will have the objective of obtaining a minimal response time so as not to impair the dynamics of the active filter

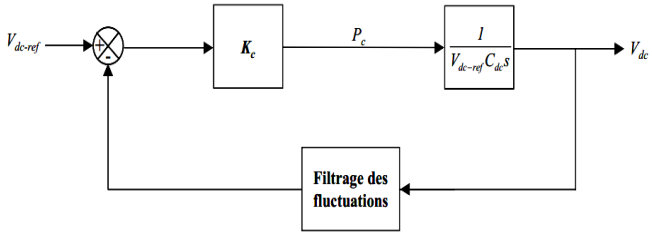

Fig. 7 The DC control loop Vdc

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D. Energie Storage

The energy storage on the DC side is often done by a capacitive storage system represented by a capacitor Cdc which plays the role of a DC voltage source Vdc. The choice of the parameters of the storage system (Vdc and Cdc) affects the dynamics and the compensation quality of the parallel active filter. Indeed, a high voltage Vdc improves the dynamic range of the active filter. Moreover, the undulations of the DC voltage Vdc, caused by the currents generated by the active filter and limited by the choice of Cdc, may degrade the compensation quality of the parallel active filter.

These fluctuations are all the more important as the amplitude of the filter current is large and its frequency is low. For this reason, it can be estimated that only the first harmonics are taken into account in the choice of the parameters of the storage system. To demonstrate this, two methods can be used.

The method of storage is based on the calculation of the energy supplied by the active filter during a half-period of the power pulsation related to the first two harmonics (5 and 7 for a Graetz rectifier bridge) [XU-94]. By choosing an acceptable ripple rate (ε), generally of the order of 5% of Vdc, the capacitance Cdc can be calculated from the following relation: $C_{dc} = \frac{V_s \sqrt{I_5^2 + I_7^2 - 2I_5 I_7 \cos(5\alpha - 7\alpha)}}{2\omega\varepsilon V_{dc}^2}$

TABLE I
SECTION HEADINGS

IV. SIMULATION AND RESULTS

This is to study the proper functioning of the proposed UPQC and to validate its efficiency, speed and good performance. In this part, under the real and sometimes exaggerated conditions of the electrical networks, several fluctuations, voltage dips and voltage harmonics are simulated using the UPQC MatlabR2009b-simulink software.

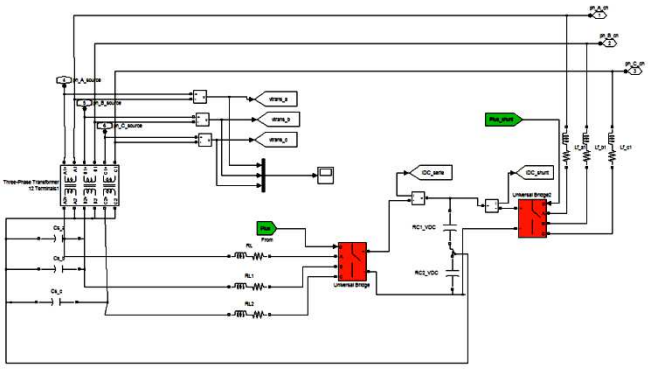

Fig. 8 Diagram of a UPQC with a serial-parallel structure

Les paramètres et les valeurs des éléments caractérisant la structure générale de l'UPQC sont donnés ci-après

Mesure	Valeur	Unite
V_s	220	V
f	50	Hz
P	8000	W
Q	500	Var
R_{line}	$0.1X10^{-6}$	Ω(Ohm)
L_{line}	$0.35X10^{-5}$	H
V_{dc}	735.6030	V
C_{dc}	0.0347	F
KI_{DC}	616.1911	/sec
KP_{DC}	4.5766	
L_f	0.0022	H
R_f	0.0200	Ω(Ohm)
KP_{shunt}	0.6183	
KI_{shunt}	757.4515	/sec
L_S	1.3842e-004	H
R_S	0.0020	Ω(Ohm)
C_S	5.2675e-005	F
$KI_{Serie\ V}$	1.9950e+003	/sec
$KP_{Serie\ I}$	0.0427	
$KI_{Serie\ I}$	52.4701	/sec

A. Compensation for frequency fluctuation

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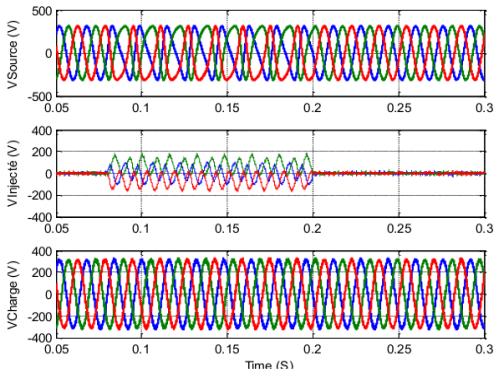

Fig. 9 Voltage of source and Load

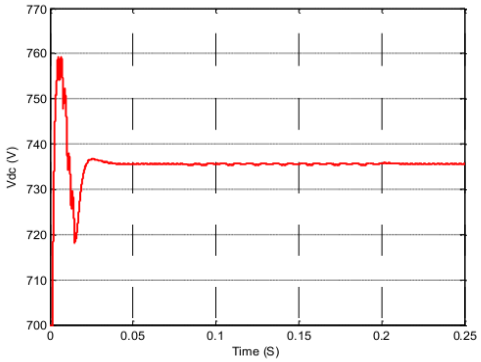

Fig. 10 Voltage Vdc by the regulator PI

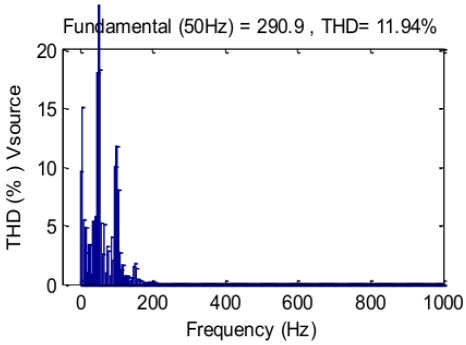

Fig. 21 Load THD spectrum

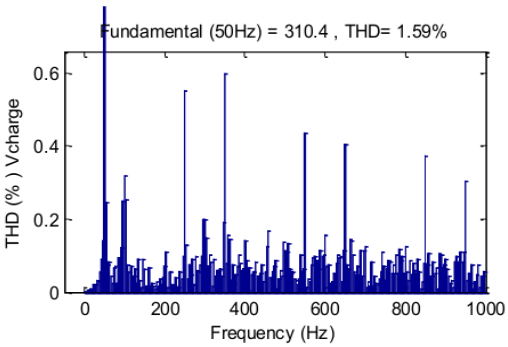

Fig. 32 The source voltage THD spectrum

B. Voltage Density Compensation

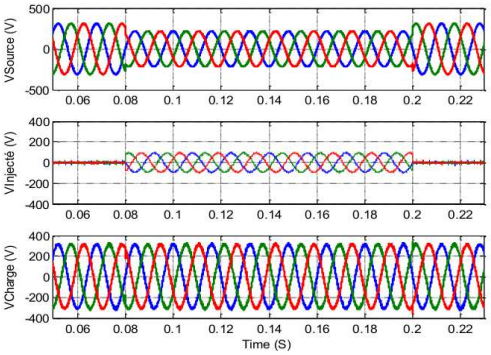

Fig. 43 The load and source voltage

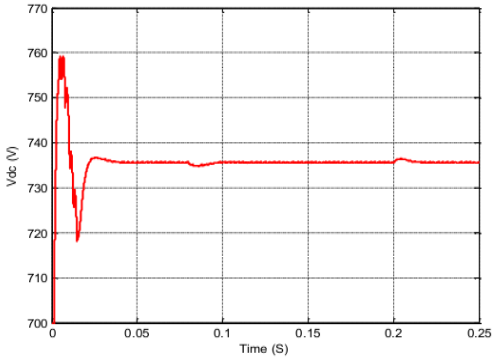

Fig. 54 The voltage Vdc by the regulator PI

C. Short cut compensation

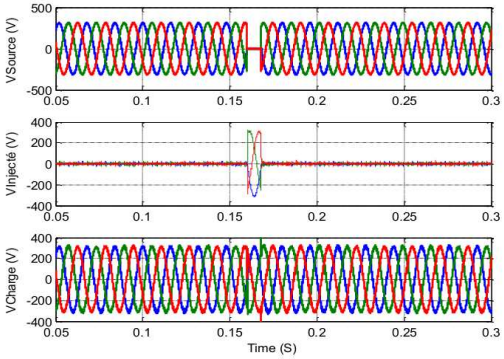

Fig. 65 The load and source voltage

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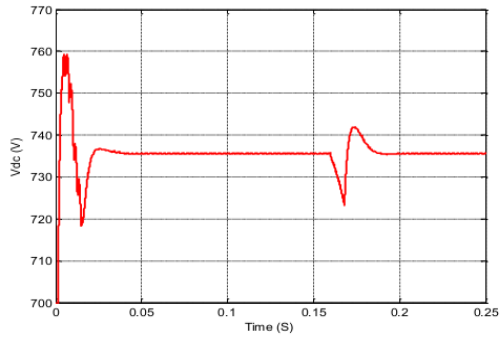

Fig. 76 The voltage Vdc by the regulator PI

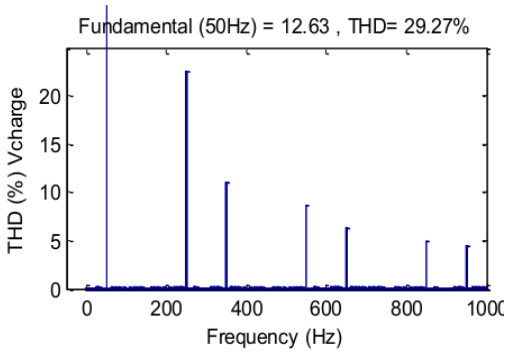

Fig. 109 Load voltage THD spectrum

D. Voltage harmonic compensation

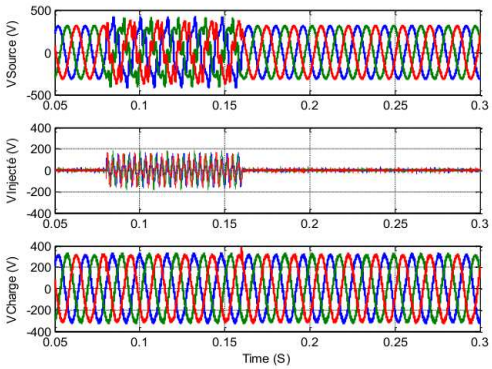

Fig. 87 The Load and source voltage

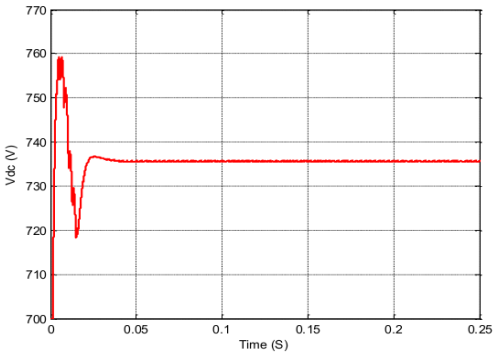

Fig. 98 The voltage Vdc by the regulator PI

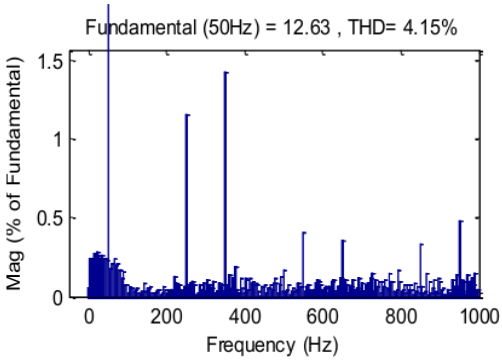

Fig. 20 The source voltage THD spectrum

Figures (3), (13), (15) and (17) represent the load voltage with the perturbation, the voltage injected by the UPQC to correct the fault and the source voltage after the disturbance compensation.

Figures (10), (14), (16) and (18) represent the bus voltage Vdc.

Figures (11), (12), (19) and (20) represent the source voltage THD spectrum and the load. As seen as the 11.94% load THD (11) is reduced after the compensation in the stroke fig (12).

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V. CONCLUSIONS

This work can be a platform for research to further assess the importance of these active filters in the field of electrical energy quality, where we can recommend the use of artificial intelligence for the regulators used in The different commands in the UPQC.

The results of the simulations carried out in this work showed the efficiency and the capacity of the UPQC to adapt and to compensate the maximum disturbances that can appear in the electrical network.

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