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Modelling and implementation a new five-level inverter topology

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***Abstract*— Nowadays multilevel inverters are most popularly used in high power and high voltage applications; they convert DC power to AC power at required output voltage and frequency level. Conventional multilevel inverter topologies include diode clamped multilevel l inverter, flying capacitor multilevel inverter and cascaded H bridge multilevel inverter. The main limitations of the conventional topologies are large number of switches. This article treats the design and realization of a new five-level single-phase inverter structure controlled by a microcontroller-based digital strategy. The proposed topology needs less number of switches and carrier signals and THD of the proposed topology is less compared to conventional topologies. All circuits are modeled and simulated using Matlab-Simulink software and ISIS proteus**

***Keywords*— photovoltaic, multilevel inverter, five-level, harmonic distortion rate TDH, Matlab-Simulink, ISIS proteus**

I. INTRODUCTION

In the last few decades, multilevel voltage-source inverters have expected much attention because of their major advantages and emerged as a viable solution for high-power dc-to ac conversion applications [1-2]. Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved.

A multilevel inverter (MLI) is a linkage structure of multiple input dc levels (obtained from dc sources and/or capacitors) and power semiconductor devices to synthesize a staircase waveform [3].

Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped) [4]; capacitor-clamped (flying capacitors) [5-7]; and cascaded multi cell with separate dc sources [5], [8-9].

In multilevel converter, the power quality is improved as the number of levels increase at the output voltage. However, it increases the number of switching devices and other components, increases the cost and control complexity and tends to reduce the overall reliability and efficiency of the converter.

The research on multilevel inverter is ongoing further to reduce the number of switching devices count to reduce the manufacturing cost, capacitor voltage balancing, which is the purpose of our paper.

This paper focuses mainly on the H-bridge inverter topology. This multilevel inverter has the potential to be the most reliable out of three topologies. It has the best tolerance owing to its modularity a feature that enables the inverter to continue operate at lower power levels after cells failure [2].

After having presented an introduction of multilevel inverter, we describe our proposed five-level inverter. Then, we carried out the results of simulations which are obtained in the environment Matlab-Simulink and ISIS PROTEUS. Finally, we discuss the simulation results and show an improvement in the sinusoidal waveform.

II. PROPOSED ARCHITECTURE

A. Description of the proposed architecture

Conventional cascaded multilevel inverters (Cascaded H-Bridge Five Level Inverter) [5], [8] and [9], (Diode Clamped Five Level Inverter) [4] (Flying Capacitor Five Level Inverter [5-7] require large number of switches. it doesn't need to use all the switches.

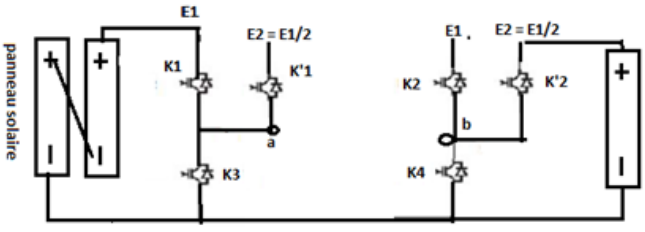

Fig. 1 Power Circuit Five Level Inverter

Fig. 1 shows a five level inverter. The converter consists of two DC sources delivered by two solar panels E1 = 36.4 V and E2 = E1 / 2 and 6 switches, each switch is composed of a

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MOSFET transistor and a diode; the MOSFET switches are used because of its fast switching capability.

B. Operation mode

The aim is to determine the values that can be taken by the output voltage ' V_{ab}' for the different possible states of the static switches, and to show the sequences of the switches conductions 't_i'.

For an N-level converter, we have N possible operating sequences to generate the N voltage levels. Particularly for five levels there are five sequences of operation.

The connection function F_{ki} translates the open or closed state of the switch k_i:

$$F_{ki=} \begin{cases} 1 \text{ if k switches is closed} \\ 0 \text{ if k switches is opned} \end{cases}$$

The look up table (Tab. 1) for the proposed inverter shows the output voltage levels and the corresponding switch states.

TABLE I
SWITCHING SEQUENCE FOR SIMPLIFIED FIVE LEVEL INVERTER

K1	k'1	K2	k'2	K3	K4	Va_Vb= Vab	t
0	0	0	0	0	0	0	t1
0	1	0	0	0	1	+E1/2	t2
1	0	0	0	0	1	+E1	t3
0	1	0	0	0	1	+E1/2	t4
0	0	0	0	0	0	0	t5
0	0	0	1	1	0	-E1/2	t6
0	0	1	0	1	0	-E1	t7
0	0	0	1	1	0	-E1/2	t8

We have chosen a uniform sequence step i.e. $t_i = t_{i-1}$, to have a frequency equal 50Hz i.e. T = 20ms we took t_i = 2.5ms.

Figure 2 shows the waveform of the voltage obtained at the inverter output.

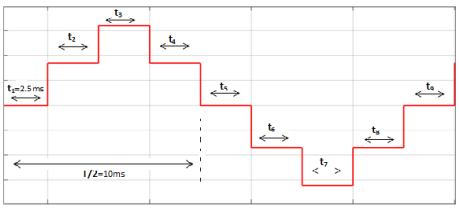

Fig. 2 Typical output voltage waveform of a multilevel inverter

III. SIMULATION AND RESULTS

In order to verify the proposed inverter, we have implemented the inverter power system in the MATLAB/SIMULINK environment and equally, under the ISIS proteus software for a practice implementation.

A. MATLAB simulation

We proposed in Fig. 3, the inverter power system which is composed by six MOSFET switches. Each switch is controlled by the adequate pulse sequence in order to product wave voltage with five levels and of 50 Hz frequency. The input supply for each DC source is respectively 34.6V and 17V. During this phase of simulations, we have implemented the multilevel inverter only in the MATLAB/SIMULINK environment.

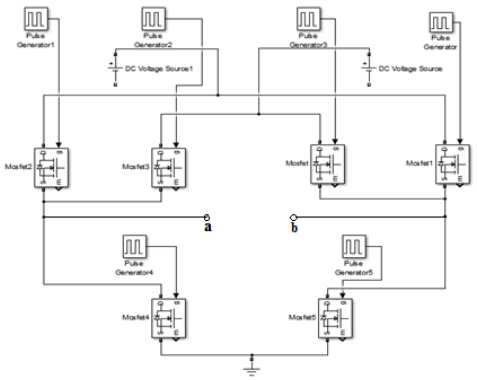

Fig. 3 Power Circuit Five Level Inverter

. The outputs of an inverter (voltage, current) contain certain harmonics, and the quality of the energy supplied by an inverter is evaluated according to the parameter calculation of total harmonic distortion THD.

Fig. 4 shows the output waveform before output LC filter and the THD response of the proposed inverter. As shown in Fig. 4, Waveform near to sine wave is achieved due to switching devices in series of DC voltage which helps us to achieve output sine waveform with minimum inductor in output filter.

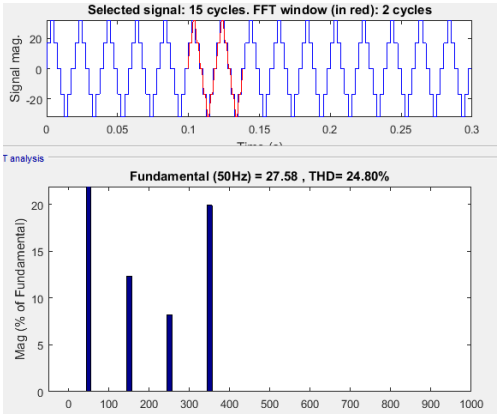

Fig. 4 Output voltage of proposed five level inverter and THD response

For the filtering we used the LC filter (Fig. 5) which allows decreasing the harmonics around the switching frequency.

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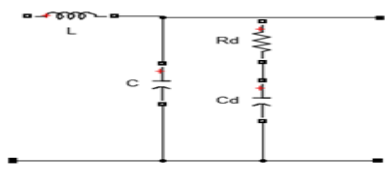

Fig. 5 LC filter

The filtered voltage and THD response of the proposed converter are shown in Fig. 6.

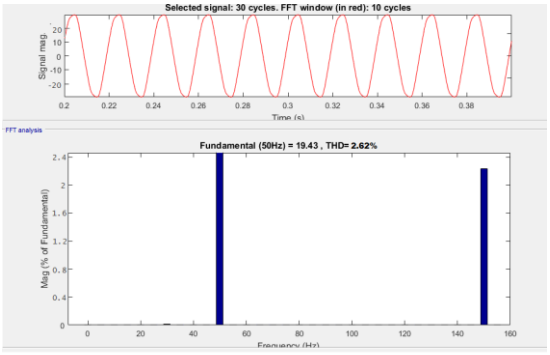

Fig. 6 Output voltage of proposed five level inverter and THD response

The THD of five level voltages is 26.86% and filtered voltage is 2.62%.

B. *ISIS PROTUS simulation*

After having performed simulations using Matlab software, the next stage was simulated using Proteus ISIS software.

1. *Control circuit*

Control interface part consists of two BLOCS: The first bloc transfers the control signals calculated by the control part to the power converters. We chose to use a microcontroller PIC16F877A to perform this part because of its small footprint, low energy consumption and also This microcontroller is selected for the construction of prototype by considering the availability of the microcontroller as well as the easiness in writing the program codes for generating pulses.

The second block includes an isolation stage between the power parts and the low power part. It is provided by optocouplers to protect the control part in case of failure (Fig .7).

In addition this block makes it possible to inject a strong current into the grid of the switch since, the grid of the MOSFET switch requires a strong current to charge these parasitic capacitances in brief time.

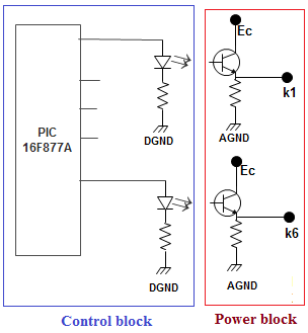

Fig. 7 Control circuit

Therefore, we have two distinct ground: a) AGND mass which is the power mass, b) DGND mass which is the control mass.

In the proposed inverter (Fig. 1) the 4 upper MOSFET switches K_1 K'_1 K_2 K'_2 operate in floating mode, i.e. their sources are not connected to the AGND mass, so to saturate the switches it is necessary to ensure that:

Voltage VGS >6V which give VG> Vs+ 6

2. *Implementation of the proposed inverter*

Schematic circuit for simulation using Proteus ISIS software can be seen in Fig. 8.

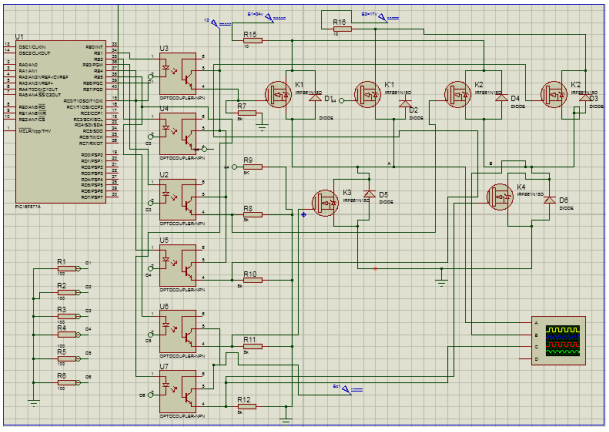

Fig. 8 Overall schematic system for simulation using Proteus Software

In ISIS Proteus software, the microcontroller circuit is connected to the inverter circuit, to control the switches by using a binary code based on C language. The output signal of microcontroller resulted with Proteus software is as shown in Fig. 9.

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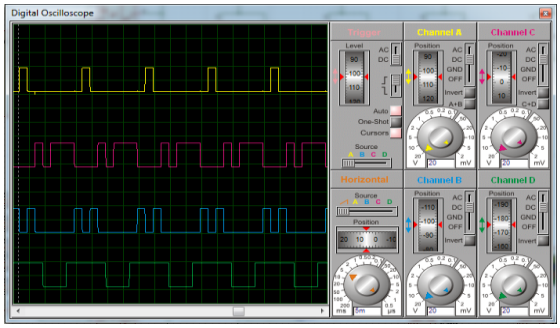

Fig. 9 Pulses of control circuit

Fig. 10 shows the resulted output voltage of the inverter, measured at a frequency of 50 Hz.

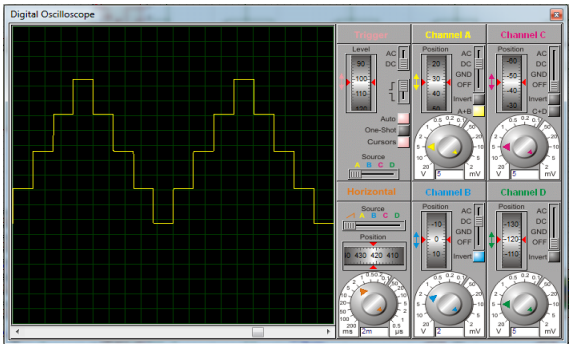

Fig. 10 Output phase voltage of proposed 5 level inverter

IV. FUTURE SCOPE

The THD of the multilevel inverter can be further reduced by using another control technique a sinusoidal pulse width modulated (SPWM) which will be generated by the microcontroller, the microcontroller is programmed to generate two digital signals: a sinusoidal signal with a frequency of 50Hz and a high frequency triangular signal. These two signals will be compared with each other, and the desired SPWM signal will be giving in the comparator output. This last will be multiplexed by a multiplexer 1 of 8 (circuit 4051), in order to control the 6 MOSFETs. The choice of the switch is ensured by the address bits (a0, a1, a2) (Fig. 11).

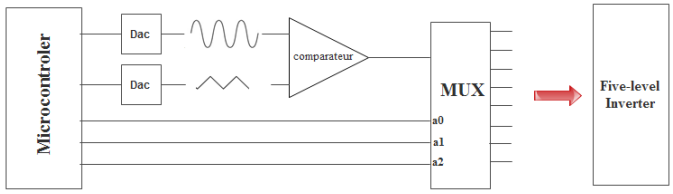

Fig. 11 Generated signal SPWM circuit

V. CONCLUSIONS

Multilevel inverters have been used in many industrial applications like HVDC, FACTS, EV, PV systems, UPS and industrial drive applications. A novel multilevel topology is proposed in this paper. The simulation of the five-level multilevel inverter is successfully done using **control circuit.** The proposed topology significantly reduces the number of switching devices count, the manufacturing cost and capacitor voltage balancing. Simulation results shows that the proposed converter topology generates a high-quality output voltage waveform with lower order THD of output voltage.

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