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Modeling and Evaluation of Bandpass ΣΔ Modulator Non-Idealities Using Simplorer VHDL-AMS

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***Abstract*— This paper describes an implementation of a band-pass sigma-delta modulator behavioral model with SIMPLORER VHDL-AMS. The model includes most of the non-idealities which affect the performance of the component, such as sampling jitter, kT/C noise and operational amplifier parameters. A comparison with another model, implemented with MATLAB®-SIMULINK by Brigati et al., is made to highlight and validate the proposed model. The spectrum plot and the Power Spectral Density of the output signal is also presented to evaluate the characteristics of the modulator. Simulation results obtained using a second-order band-pass sigma-delta modulator demonstrate the validity of the model by the mean of estimating signal-to-noise and distortion ratios.**

***Keywords*— Sigma Delta Analog-Digital Converter; Band-pass Modulator; Simplorer VHDL-AMS; Power Spectral Density; Non-idealities Effects.**

I. Introduction

Analog-to-digital converters based on sigma-delta modulators are the most suitable converters for communication systems, audio and high resolution precision industrial measurement applications. The key feature of these converters is that they are the only low cost conversion devices which provide both high dynamic range and flexibility in converting low bandwidth input signals. A sigma-delta A/D Converter consists of an analog block (modulator) and a digital block (decimator). The use of a modulator is done in order to sample input signal at oversampling rate which generates an output stream of 1 bit. Furthermore, in order to simulate any ΣΔ A/D converter based system, developers need tested and well-suited models to evaluate the performance of their systems on different development software platform such as MATLAB-SIMULINK and SIMPLORER VHDL-AMS [1]–[4].

Therefore, and in order to enrich the behavioral model libraries of SIMPLORER VHDL-AMS, a behavioral model of second order band-pass sigma-delta modulator is proposed and discussed. The model takes into account most of non-idealities such as sampling jitter, kT/C noise and operational amplifier parameters. We also analyze the behavior of the modulator in two case studies: ideal and non-ideal. Finally, simulation results obtained from the proposed model are compared with those obtained from the model proposed by Brigati et al. for MATLAB®-SIMULINK [5].

II. Sigma-Delta ADC Converter

A sigma-delta converter consists of an integrator, a comparator and a single bit digital-to-analog converter (DAC), as shown in Fig. 1. The output of the DAC is subtracted from the input signal. The resulting signal is then integrated, and the integrator output voltage is converted to a single-bit digital output by the comparator. The resulting bit becomes the input of the DAC and the latter's output is subtracted from the ADC input signal and so on. This closed-loop process is carried out at a very high "oversampled" rate. The digital data coming from the ADC is a stream of "ones" and "zeros," and the value of the signal is proportional to the density of digital "ones" coming from the comparator. This bit-stream data is then digitally filtered and decimated to in a binary-format output [6].

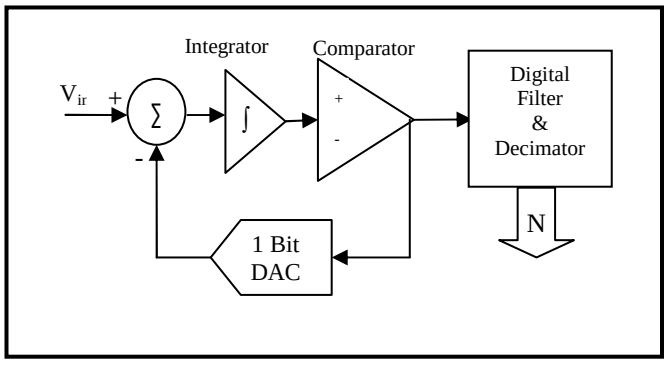

Fig. 1 Sigma-Delta A/D converter architecture.

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III. Simulation Results of Ideal Band-Pass Sigma-Delta ADC with VHDL-AMS.

Band-pass sigma-delta modulators are representing the reference front-end architecture for Amplitude Modulation (AM), Quadrature Amplitude Modulation (QAM) and Frequency Modulation (FM) systems. To describe the behavior of such modulators, we used a powerful development environment: SIMPLORER VHDL-AMS. It is an intuitive, multi-domain, multi-technology simulation program that enables developers to simulate complex power electronic and electrically controlled systems [7]. The bloc diagram of ideal second order band-pass sigma delta modulator implemented with SIMPLORER is given in Fig. 2. The parameters values chosen for simulation are summarized in Table I.

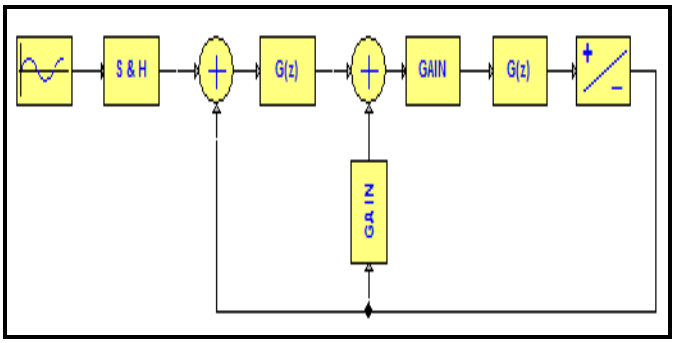

Fig. 2 Simulated ideal model in SIMPLORER VHDL-AMS.

TABLE I
Simulation Parameters.

Parameters	Value
Amplitude Signal [V]	0.5
Frequency Signal [Hz]	BW = 500
Sampling frequency [kHz]	Fs = 10
Samples number	N = 65536
Integrator gains	Gain1 = 0.25 Gain2 = 0.125
G(z)	$G(z) = (-z^{-2})/(1+z^{-2})$

The simulation results are obtained using the "DAY Post Processor" of SIMPLORER. It is a powerful tool to calculate new data channels. This tool includes integration, differentiation, calculation of power characteristics and the Fast Fourier Transform (FFT) of data channels [3]. Figs 3, 4 and 5, show Input/Output signals implemented with SIMPLORER, spectrum plot of the output signal and the Power Spectral Density of the ideal modulator.

The performance of sigma-delta modulator can be affected by a set of non idealities such as sampling jitter, KT/C noise and operational amplifier parameters (noise, finite gain, finite bandwidth, slew rate and saturation voltages). Fig. 6 shows the block diagram of a second order band-pass sigma-delta modulator implemented using the proposed SIMPLORER models.

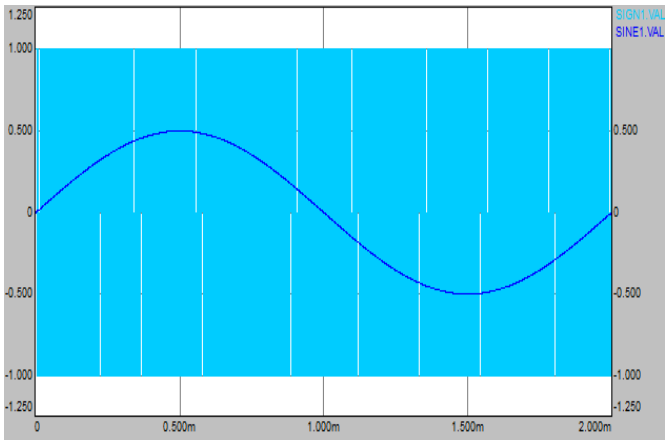

Fig. 3 Input and output waveform implemented with "Day Post Processor" option of SIMPLORER.

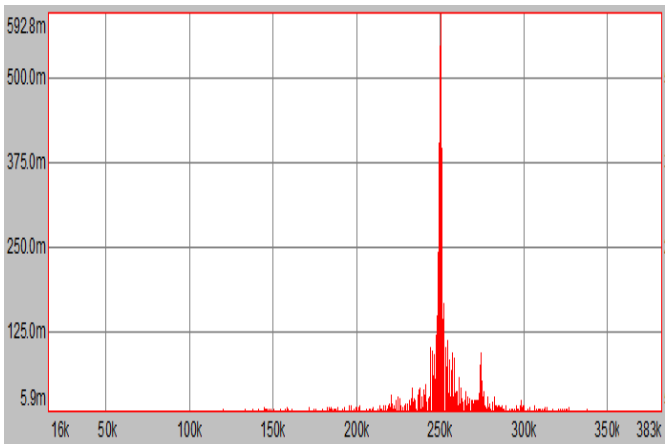

Fig. 4 Spectrum plot output signal with "Day Post Processor" option of SIMPLORER.

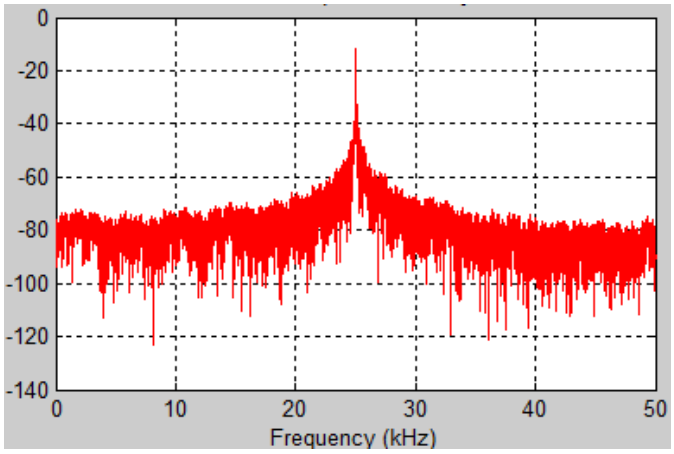

Fig. 5 Power Spectral Density of ideal bandpass sigma-delta modulator.

To validate the models proposed of the various non-idealities affecting the operation of the band-pass sigma-delta modulator, we performed several simulations with VHDL_AMS Simulator where only the non-idealities of the

first resonator were considered, since their effects are not attenuated by the noise shaping. The parameters values chosen for the simulation are summarized in Table II.

Simulation results are given in Figs 7 and 8. It is clear that non-idealities errors affect the performances of the modulator. Harmonics of spectrum plot for real modulator are more distributed than the ideal model, so it affects the measurement of total harmonic distortion (THD) of the modulator.

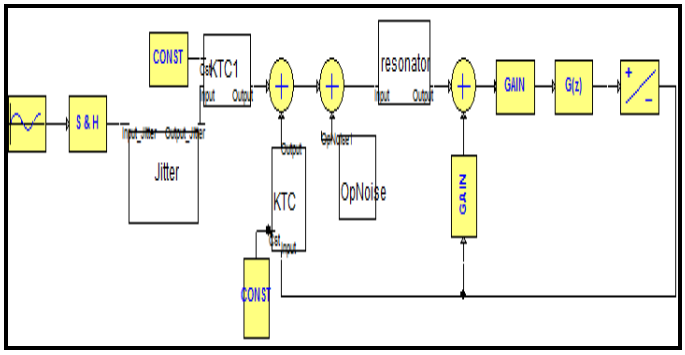

Fig. 6 Block diagram of a second-order sigma-delta modulator.

TABLE II
SIMULATION PARAMETERS

Parameters	Value
Amplitude Signal [V]	0.5
Frequency Signal [Hz]	BW = 500
Sampling frequency [kHz]	Fs = 10
Samples number	N = 65536
Integrating Capacitance of the first integrator	C=4E-12
Integrator gains	Gain1 = 0.25 Gain2 = 0.125

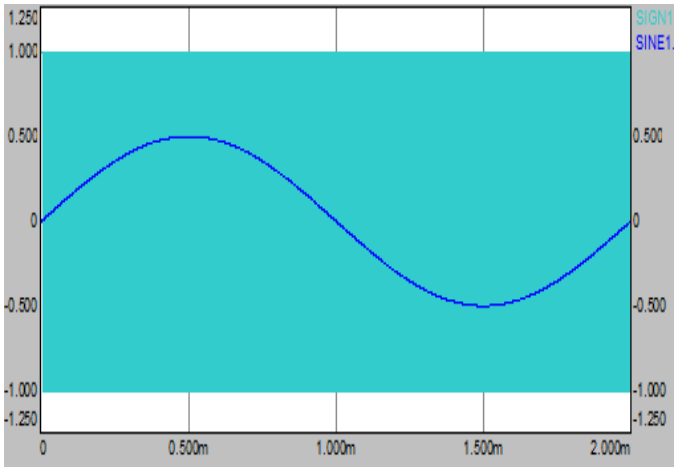

Fig. 7 Input/output waveform implemented with the "Day Post Processor" option of SIMPLORER of real band-pass sigma-delta modulator.

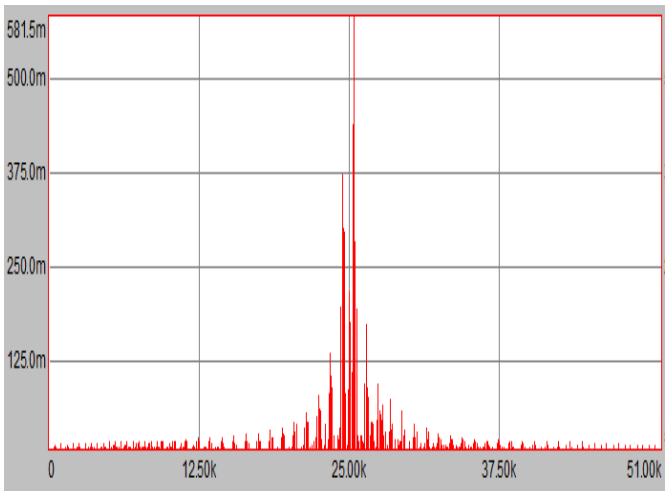

Fig. 8 Spectrum plot of output signal with non-idealities.

IV. OVERVIEW OF NON-IDEALITIES MODELS IMPLEMENTED WITH SIMPLORER VHDL-AMS

In this section, we detail models of different errors added to the band-pass sigma-delta modulator: sampling jitter, kT/C noise and Op-Amp Noise.

A. Sampling clock Jitter

Sampling clock jitter results in non-uniform sampling, it increases the total error power in the output quantizer. Fig. 9 shows the behavioral model of the clock jitter implemented with SIMPLORER.

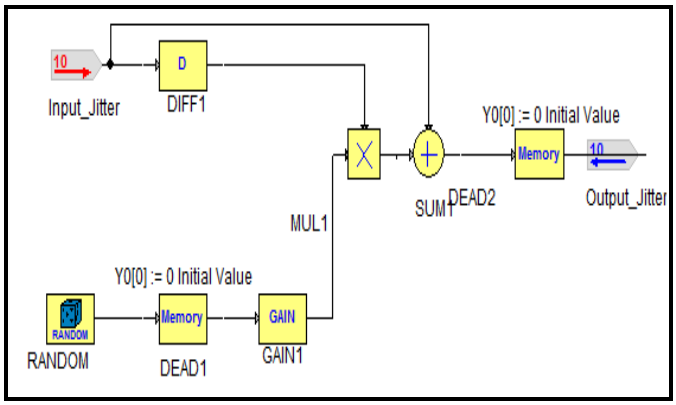

Fig. 9 Modeling of clock jitter with SIMPLORER.

B. Op-Amp Noise

Fig. 10 shows the model of the op-Amp noise implemented with SIMPLORER.

C. Thermal Noise

Thermal noise is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium. Thermal noise has a white spectrum and wide band limited only by the time constant of the switched capacitors or the bandwidths of op-amps [7]. Fig. 11 shows behavior model on SIMPLORER of KT/C noise.

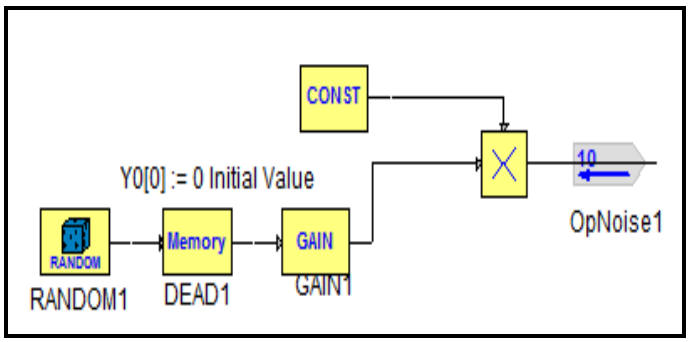

Fig. 10 Modeling of Op-Amp Noise with Simplorer.

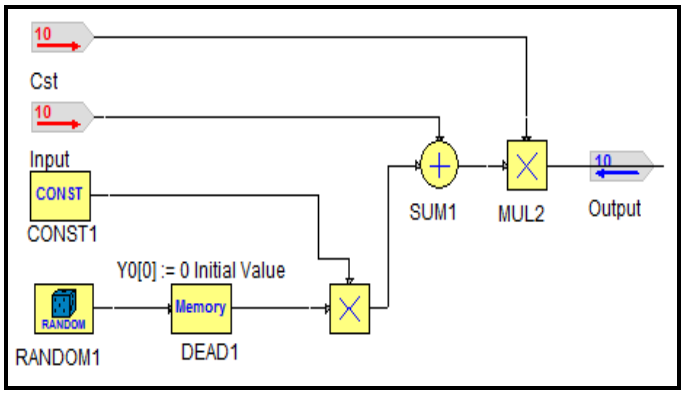

Fig. 11 Modeling of Thermal Noise with Simplorer.

V. Comparison and Validation of the Proposed Model

To evaluate results obtained with SIMPLORER, we rely on MATLAB®-SIMULINK model of the band-pass sigma-delta modulator developed by Brigati et al [5]. Fig. 12 shows the block diagram of the modulator implemented with SIMULINK which contains the most significant non-idealities of a sigma-delta modulator.

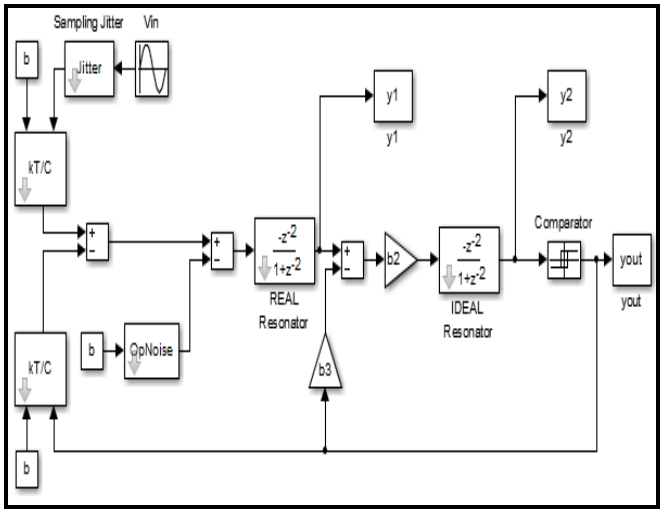

Fig. 12 Block diagram of a second-order band-pass sigma-delta modulator implemented using the proposed SIMULINK models [5].

Figs 13 and 14 present the spectrum plot of the output signal implemented with SIMULINK and SIMPLORER. The baseband power spectral densities of the band-pass ΣΔ output bit-stream obtained with SIMULINK and SIMPLORER are shown in Figs 15 and 16.

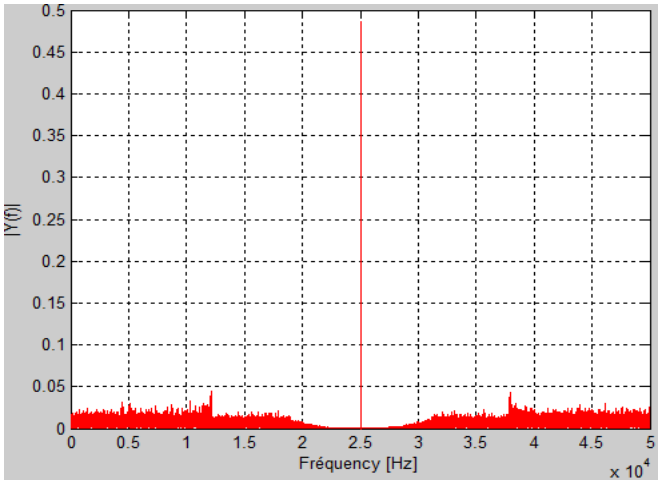

Fig. 13 Spectrum plot of output signal with SIMULINK.

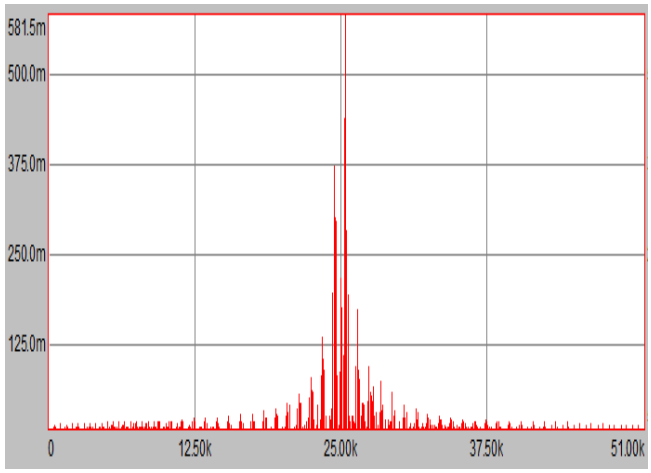

Fig. 14 Spectrum plot of output signal with SIMPLORER.

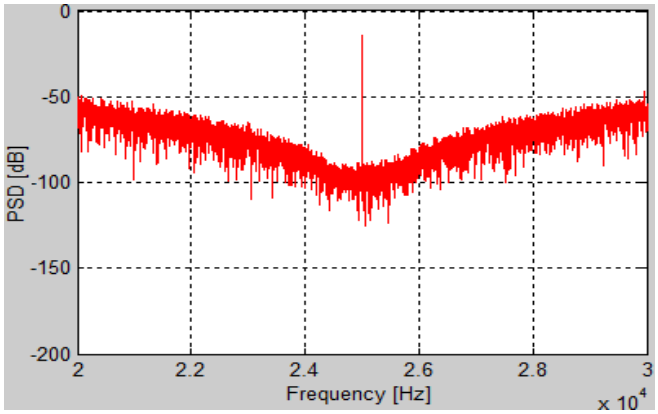

Fig. 15 PSD of band-pass Sigma-Delta modulator obtained with SIMULINK.

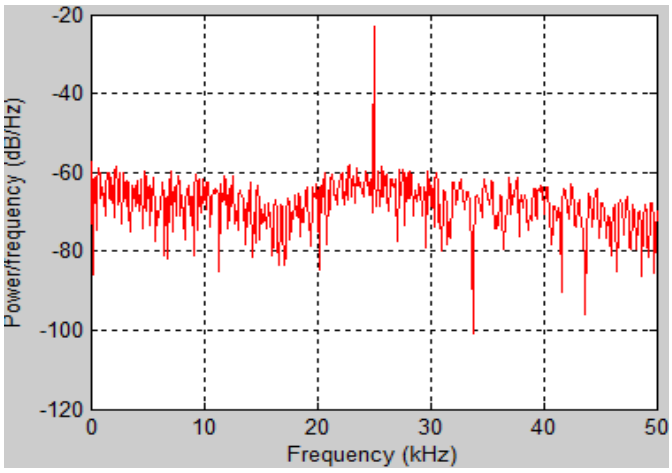

Fig. 16 PSD of band-pass sigma-delta modulator obtained with SIMPLORER.

Measurement results obtained in [5], note that SNDR is equal to 57.2 dB and with the proposed model implemented in SIMPLORER, we note that SNDR is equal to 56.9. So, results obtained with SIMPLORER are very close to those obtained with SIMULINK. This result permits the validation of the proposed model.

VI. Conclusion

In present work, we presented a complete set of behavior model of second order band-pass Sigma-Delta modulator including the non-idealities of modulator. We defined three macros implemented with SIMPLORER which describes the behavior of such non-idealities of the modulator: Clock Jitter, Thermal Noise and operational amplifier Noise. A simulation result of PSD measurement was presented and a comparison with SIMULINK model was made to validate our model.

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