Proceedings of Engineering & Technology (PET)
pp. 604-609

Low power consumption, low phase noise ring oscillator in 0.18 µm CMOS process

Nadia Gargouri, Dalenda Ben Issa, Zied Sakka, Abdennaceur Kachouri & Mounir Samet

Laboratory of Electronics and Technologies of Information (LETI)
National School of Engineers of Sfax B.P. 1173, 3038 Sfax
University of Sfax - Tunisia

gargourinedia@hotmail.fr
dalenda_benissa@yahoo.fr
sakka_zied@yahoo.fr
abdennaceur.kachouri@enis.rnu.tn
mounir.samet@enis.rnu.tn

***Abstract*— In this work, a new ring voltage controlled oscillator with a two cross coupled load PMOS transistors is proposed. The proposed method preserves the maximum frequency of the VCO unaffected which leads to improvement in phase noise and the power consumption of VCO oscillators.**
The proposed ring oscillator implemented in 0.18µm CMOS shows the worse phase noise of -108 dBc/Hz at 10MHz offset, tuning range of 140.7%, while dissipating a maximum power consumption of 9 mW from 1.8 V supply.

***Keywords*— Ring oscillators, VCO, tuning range, phase noise, cross coupled PMOS transistors.**

I. INTRODUCTION

Ultra-wide band (UWB) is a very promising technology for short-range and low data rate wireless communications. This enormous growth began since 2002 when the American Federal Communications Commission (FCC) released the use of a 7.5 GHz band spectrum (3.1–10.6 GHz) with a power spectral density of -41.3 dBm/MHz [1].

Impulse-radio ultra-wide band (IR-UWB) is a relatively new trend in UWB communications and a promising technique that offers viable solutions to the limitations of UWB communications technology mentioned above [2]. It has attracted growing attention during the last few years due to its advantageous features and attractive properties. IR-UWB systems can be designed with relatively low-complexity and low power consumption, and have attractive specifications for imaging and radar applications [3, 4].

The oscillator is a key block in a IR-UWB system and a challenging design since it has to accommodate the defined constraints above.

To accomplish desire specifications of applications, it is necessary the VCO be designed to have wide tuning range, low phase noise, low power dissipation, simplified integration method, and small layout area

LC voltage-controlled oscillators (LC VCOs) are typically utilized in wireless transceivers due to their good phase noise performance [5], but our application demand the design with easy implementation of the circuit, small chip area, low cost and good low phase noise.

The implementation of high quality inductor and capacitor in a standard CMOS process requires extra non standard processing steps and also increases the chip area and the cost.

In contrast, ring VCOs are compatible with digital CMOS technologies and occupy small chip area. Owing to these attributes, ring VCOs are a popular candidate for implementation in scaled CMOS. Unfortunately, they exhibit poor phase noise performance due to a low Q and a large VCO-gain (Kvco)[6]. Thus, the next task is to improve the phase noise for a ring VCO.

Extensive research has been carried out to analyze and improve the phase noise of ring oscillators [7-10]. From these works, it has been reported that the phase noise of ring oscillators is degraded by the multi-path structure [7], and the alignment technique [8, 9].

The VCOs reported in [10] provides fast rail-to-rail switching, thus improving the Q of the ring VCO and lowering the phase noise. However, it suffers from an extremely narrow tuning range.

In this paper, an improved VCO operating at 1.8V supply voltage and -108 dBc/Hz at 10 MHz low phase noise is proposed. This method circuit improves the phase noise by reducing the VCO- gain (KVCO).

The paper is organized as follows. First, the design approach of the ring-VCO which includes the topology and circuit structure used in the design is presented in Section II. Section III presents the simulation results of the proposed ring oscillator. Comparisons with other published works are also provided in this section to illustrate the advantages of the proposed design. Finally, a conclusion is drawn in Section IV.

II. PROPOSED DIFFERENTIAL RING OSCILLATOR

Fig. 1 illustrates the voltage-controlled differential ring oscillator in [11] (Fig. 1) and the proposed differential VCO (Fig. 2).

The delay cell presented in [11] is composed of a differential pair of MN1and MN2 with a cross coupled load (MP1 and MP5), along with two PMOS transistors that change the current of output node to control the tuning range.

ISSN: 2356-5608

The operation of the cell can be described as follows: by changing the control voltage (Vctr) on the gate of MP3 and MP6, the charge up current of the delay cell output load is changed. Therefore its delay time and thus the frequency of the whole VCO are controlled.

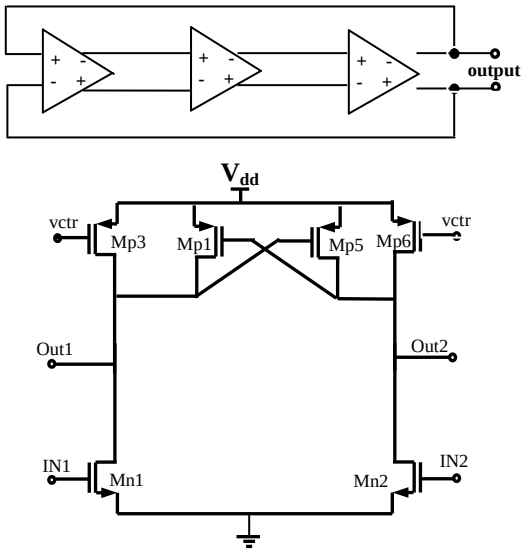

Fig. 1 the block diagram and the delay cell of the ring oscillator in ref [11]

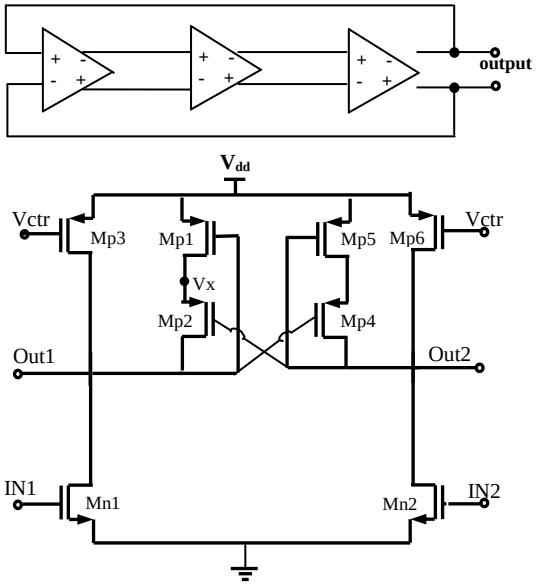

Fig. 2 The proposed differential ring oscillator.

.

Compare to Fig. 1 The proposed delay cell of ring VCO has additional MOS transistors M2 and M4 to the power supply of the two switch transistors M1 and M5, respectively.

The gates of M2 and M4 are cross-connected with the gates of M1 and M5, respectively. M2, M4 are sized corresponded to M1, M2 in order to maintain the same oscillation.

To illustrate how the phase noise is reduced in the proposed design, it is necessary to derive the operating frequency of the proposed ring oscillator. This is easily justified since the goal of our work is to show the reduced VCO-gain (kvco) of the oscillator.

The equivalent circuit of the proposed half delay cell is shown in Fig. 2.

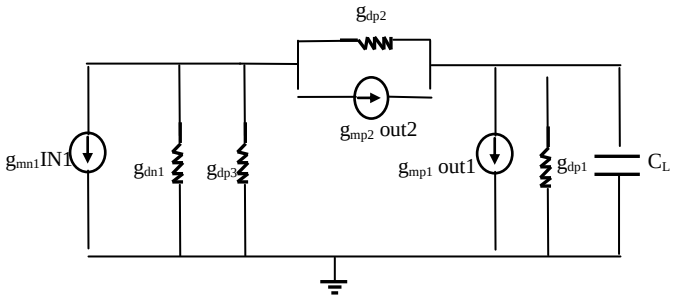

Fig.3. Equivalent circuit of the proposed half delay cell

Using Fig.3, the transfer function describing the operation of the delay cell can be approximated as:

$$H(s) = \frac{g_{mn1}}{(g_{mp1}-g_{mp2})+sC_L+g_{dn1}+g_{dp3}} \qquad (1)$$

Where g_m is the transconductance, g_d is the channel conductance and C_L is the total capacitance seen at the output node of the delay cell.

To maintain the oscillation of a ring oscillator, the overall gain is unity at the oscillation frequency. The voltage gain of the delay cell must be unity and the oscillation frequency of the ring oscillator can be derived.

$$f_{osc} = \frac{1}{2\pi}\sqrt{\frac{{g_{mn1}}^2-(g_{dn1}+g_{dp3}+g_{mp1}-g_{mp2})^2}{{C_L}^2}} \qquad (2)$$

By controlling the channel conductance gdp3 of PMOS devices Mp3, the output frequency fosc can be tuned between fmax and fmin. And the gdp3 can be expressed as:

$$g_{dp3} = \mathrm{Kpp}(\frac{W}{L})_3 V_{DD} - |V_{thp}| - V_{ctr}) \qquad (3)$$

Where $(W/L)_3$ is the width-to-length ratio of Mp3, V_{ctr} is the control voltage of the proposed ring VCO, V_{th} is the threshold voltage and Kpp is the process transconductance parameter. It is proportional to the product of the carrier mobility and the gate capacitance per unit area.

From Eq. (2), the gain of frequency tuning (KVCO) of the proposed ring oscillator can be written as:

$$K_{VCO} = \frac{1}{2\pi}\frac{\mathrm{Kpp}(\frac{W}{L})_3}{C_L}\sqrt{\frac{(g_{dn1}+g_{dp3}+g_{mp1}-g_{mp2})^2}{g_{mn1}^2-(g_{dn1}+g_{dp3}+g_{mp1}-g_{mp2})^2}} \qquad (4)$$

The equation of the KVCO of the ring oscillator in Fig.1 is given by [12].

$$K_{VCO} = \frac{1}{2\pi}\frac{\mathrm{Kpp}(\frac{W}{L})_3}{C_L}\sqrt{\frac{(g_{dn1}+g_{dp3}+g_{dp1}-g_{mp1})^2}{g_{m1}^2-(g_{dn1}+g_{dp3}+g_{dp1}-g_{mp1})^2}} \qquad (5)$$

In the proposed delay stage, gmp1 and gmp2 can be expressed as :

$$g_{mp1} = \frac{2\,I_{SD}}{V_{SGp1}-|V_{Tp}|} \qquad (6)$$

$$g_{mp2} = \frac{2\, I_{SD}}{V_{SGp2} - |V_{Tp}|} \qquad (7)$$

Where I_{SD} is the drain current through MP1 and MP2, V_{TP} is the threshold voltage, V_{SGp1} and V_{SGp2} are the source-gate voltages of MP1, MP2 respectively, which are identified as:

$$\mathbf{V_{SGp1} = V_{DD} - out_1} \qquad (8)$$

$$V_{SGp2} = V_x - out_2 \qquad (9)$$

Due to the symmetry of the differential topology, the output voltages out1 and out2 are equal in magnitude but opposite in signs. Therefore, the source-gate voltage of MP1 is greater than the source-gate voltages of MP2.

According to equations (6) and (7), gmp2 ≥ gmp1.

Based on the fact that gdp1 is much smaller than gmp1 and gmp2 is much greater than gmp1, a lower Kvco was achieved compared with that of the ring VCO in Fig.1.

Therefore, the phase noise of the proposed voltage controlled oscillator can be improved much more compared to that of the ring oscillator in [11].

Fig. 4 shows the simulated phase noise performance of the proposed voltage controlled oscillator compare to the VCO in ref [11] at the same oscillation frequency 6.9 GHz. As can be seen in Fig. 4, the phase noise of the proposed voltage-controlled oscillator improves significantly compare to that of VCO in ref [11].

The additional of MOS transistors M2 and M4 leads to additional 3dBc/Hz at 1MHz and 8dBc/Hz at 10MHz improvement in phase noise.

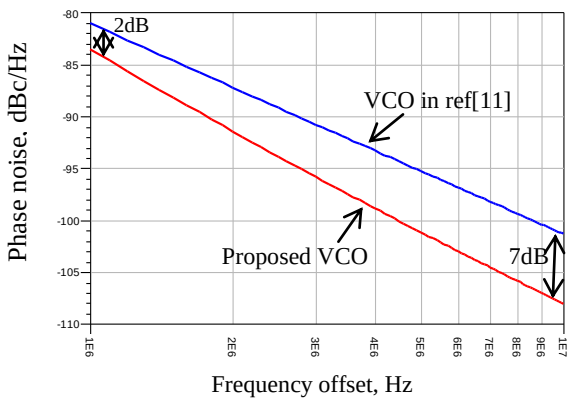

Fig.4 Simulated phase noise performance in comparison with the ring VCO in ref [11]

III. SIMULATION RESULTS

The analysis conclusions are verified by using Advanced Design System simulator. The simulations results are based on 0.18µm CMOS process.

Fig. 5 shows the graph of Output frequency versus the control voltage of VCO. When the control voltage is varied from 0V to 1.8V the Oscillation frequency of the designed VCO ranges from 6.9 GHz to 1.2 GHz.

It can be seen from this figure that the Gain (KVCO) of the proposed design is 377.13 MHz/ V which is lower than the KVCO of the ring oscillator in ref [11] that confirms the previous analysis.

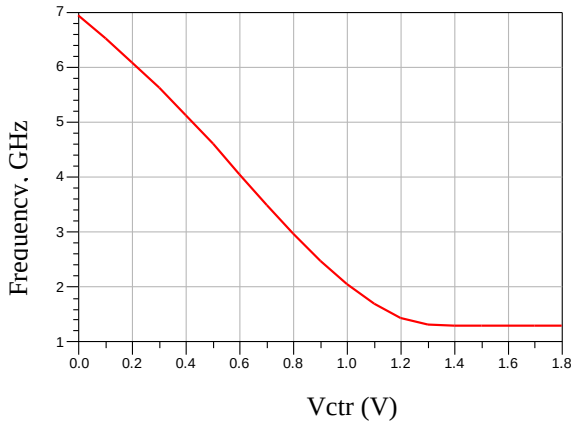

Fig.5 Oscillation frequency of the proposed oscillator versus the control voltage

Fig. 6 shows the simulated results of phase noise of the proposed ring VCO. When the oscillation frequency is 6.9GHz, the phase noise is -108dBc/Hz at 10MHz.

The output power variation is from 9mW to 0.941mW while the control voltage was tuned from 0 to 1.8 Vas shown in Fig. 7

For the same process, supply voltage and oscillation frequency (6.9GHz), the circuit of [11] has a maximum power consumption of 9.32mW.

In contrast, the proposed ring oscillator has a maximum power of 9mW, which indicates a 3.43% improvement in maximum power consumption when compared to [11].

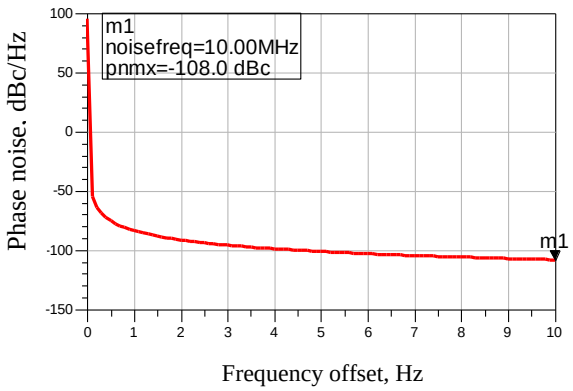

Fig.6 simulated phase noise at 6.9 GHz of the proposed ring oscillator

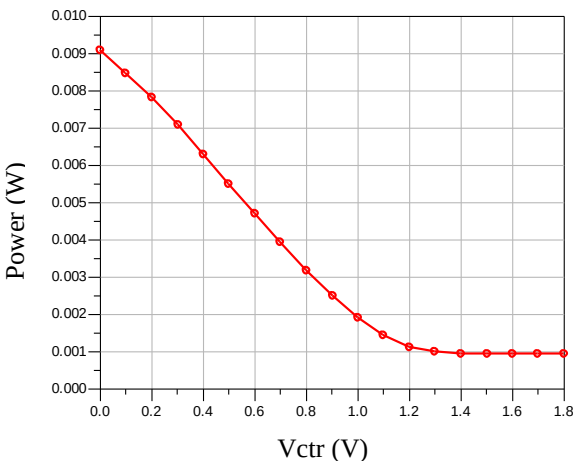

Fig.5 The output power consumption versus the control voltage

The simulation results demonstrate the improvement of the maximum power consumption by the proposed design. It can be seen that the proposed VCO can simultaneously achieve low phase noise, low power dissipation at the same frequency (6.9GHz) compare to [11].

Table 1 summarizes the overall performance of the proposed ring VCO in comparison with previously reported differential ring VCOs.

In order to provide a fair comparison with other reported works at different frequencies and power consumptions, a Figure-of-Merit (FoM) is used [13]:

$$\text{FOM} = \text{L}(\text{f}_{\text{osc}}) - 20\log\frac{\text{f}_{\text{osc}}}{\text{f}_{\text{off}}} + 10\log\frac{\text{P}_{\text{dc}}}{1\text{mw}} \qquad (9)$$

Where f_{osc} is the oscillation frequency, f_{off} is the frequency offset, $L(f_{osc})$ is the phase noise at f_{osc} , P_{dc} is the dc power consumption in mW

Based on this calculation, the figure of merit (FOM) of this proposed VCO is about –155.25 dBc/Hz at the frequency of 6.9 GHz.

From the table, it is clear that our proposed oscillator is able to achieve in overall better results compared to some of the previously reported ring oscillator designs.

IV. Conclusions

In this paper, the new configuration of differential voltage controlled oscillator with low phase noise and low power consumption is presented.

The simulations results show that the worse phase noise is –108 dBc/Hz at 10 MHz offset frequency and the maximum power consumption is about 9mW. The tuning range is about 140.7% from 6.9 GHz to 1.2 GHz and the FOM of the VCO is about –155.25 dBc/Hz.

The performance of our work is good for low power consumption and low phase noise applications such as ultra-wideband systems.

TABLE 3 : SUMMARIZED RESULTS

Results	[14]	[15]	[16]	This work
Technology	0.18µm	45nm	0.18µm	0.18µm
fosc (GHz)	2.45	11.5	4.09	6.9
Tuning range (GHz)	12.87%	95.6%	88%	140.7%
P (mW)	6.99	3	13	9
Phase noise (dBc/Hz)	-112 @10MHZ	- 78 @10MHz	- 93.3 @1MHz	-108 @10MHz
FOM (dBc/Hz)	-151.33	- 134.44	- 154.39	- 155.25

References

[1] Federal Communications Commission, FCC notice of proposed rule making, revision of part 15 of the commission's rules regarding ultra-wideband transmission system, FCC, Washington DC, ET-docket 98-153

[2] Bassem Fahs, Walid Y. Ali-Ahmad and Patrice Gamand, *A Two-Stage Ring Oscillator in 0.13-µm CMOS for UWB Impulse Radio*, IEEE Transcations on Microwave Theory and Techniques, Vol. 57, N°. 5, May 2009.

[3] K. Chen, *Linear Networks and Systems* (Book style). Belmont, CA: Wadsworth, 1993, pp. 123 135

[4] H. Poor, *An Introduction to Signal Detection and Estimation*. NewYork: Springer-Verlag, 1985, ch. 4

[5] Hai Feng Zhou, Kam Man Shum, Ray C. C. Cheung, Quan Xue and Chi Hou Chan, *A Low power low phase noise LC voltage controlled oscillator*, Progress In Electromagnetics Research Letters, Vol. 38, pp.65-73, 2013.

[6] Razavi, B, A *study of phase noise in CMOS oscillators*, IEEE Journal of Solid-State Circuits, Vol. 31, pp. 331-343,1996.

[7] Straayer MZ and Perrott MH, *A multi-path gated ring oscillator TDC with first-order noise shaping*, IEEE Journal of Solid-State Circuits, April 2009.

[8] Shieh Ali Saleh S and Masoumi N, The dual-edge alignment technique with improved spur reduction effects in ring oscillators. Microelectronics Journal, 2011, doi:10.1016/j.mejo.2011.04.002.

[9] Ye S, Jansson L and Galton I, *A multiple-crystal interface PLL with VCO realignment to reduce phase noise*, In: Proceedings of the IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers. 2002. p. 78447-

[10] Joo-Myoung Kim, Seungjin Kim, In-Young Lee, Seok-Kyun Han, and Sang-Gug Lee, *A Low-Noise Four-Stage Voltage-Controlled Ring Oscillator in Deep-Submicrometer CMOS Technology*, IEEE transactions on circuits and systems—II: EXPRESS BRIEFS, VOL. 60, N°. 2, pp. 71-75, February 2013.

[11] Xuemei Lei, Zhigong Wang, Lianfeng Shen, and Keping Wang, *A Large Tuning Range Ring VCO in 180nm CMOS*, Progress In Electromagnetics Research Symposium Proceedings, March 2013.

[12] Lei Xuemei, Wang Zhigong and Shen Lianfeng, *Design and analysis of a three - stage voltage - controlled ring oscillator*, Journal of Semiconductors, Vol. 34, No 11, November 2013.

[13] Oleg Nizhnik, Ramesh K. Pokharel, Haruichi Kanaya, and Keiji Yoshida, *Low Noise Wide Tuning Range Quadrature Ring Oscillator for Multi-Standard Transceiver*, IEEE Microwave and Wireless Components Letters, vol. 19, N° 7, July 2009.

[14] Jubayer Jalil, Manum Bin Ibne Reaz, M. A. M. Ali and T. G. Chang, *A Low Power 3-Stage Voltage-Controlled Ring Oscillator in 0.18 µm CMOS Process for Active RFID Transponder*, ELEKTRONIKA IR ELEKTROTECHNIKA, Vol.19, N°.8, 2013.

[15] Shivalal Patro, J.K. Panigrahi and Sushanta K. Mandal, *A 6–17 GHz linear wide tuning range and low power ring oscillator in 45nm CMOS process for electronic warfare,* International Conference on Communication, Information & Computing Technology (ICCICT), 2012.

[16] Meng-Lieh Sheu, Yu-Shang Tiao and Lin-Jie Taso, *A 1-V 4-GHz wide tuning range voltage-controlled ring oscillator in 0.18μm CMOS*, Microelectronics Journal,Vol. 42, N°6, Juin 2011.