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Evaluation of Non-Idealities Effects Implemented in a Cascade-Of-Integrator-FeedBack Sigma-Delta Modulator Model using Simplorer VHDL-AMS

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***Abstract*— This paper describes an implementation of a "Cascade-of-Integrator-FeedBack" (CIFB) Sigma-Delta modulator behavioral model in SIMPLORER VHDL-AMS. The model includes most of the non-idealities which affect the performance of the component, such as sampling jitter, KT/C noise and operational amplifier parameters. The spectrum plot and the Power Spectral Density of the output signal is also presented to evaluate the characteristics of the modulator. Simulation results obtained using a second-order CIFB Sigma-Delta modulator demonstrate the validity of the model by the mean of estimating signal-to-noise and distortion ratios and effective number of bits.**

***Keywords*— Sigma Delta Analog-Digital Converter; CIFB Modulator; Simplorer VHDL-AMS; Power Spectral Density; Non-idealities Effects.**

I. Introduction

Nowadays mixed signal circuits are filling the gap between analog and digital circuits which reduces the size of system, increases speed of operation, reduces power dissipation and increases design flexibility. Data converters are the core components of the mixed signal systems [1]. Analog-to-digital converters based on sigma-delta modulators are the most suitable converters for communication systems, audio and high resolution precision industrial measurement applications. The key feature of these converters is that they are the only low power and low cost conversion devices which provide both high dynamic range and flexibility in converting low bandwidth input signals. Sigma Delta ADC, a type of oversampling ADC is highly tolerant to analog circuit imperfections, thus making it a good choice to realize embedded ADC interfaces in modern systems-on-chip (SoCs) [2]. In addition to their tolerance for circuit non idealities, over-sampled A/D converters simplify system integration by reducing the burden on the supporting analog circuitry. Because they sample the analog input signal at well above the Nyquist rate, precision sample-and-hold circuitry is unnecessary. Also, the burden of analog anti-aliasing filter is considerably reduced. Much of its function is transferred to the digital decimation filter, which can be designated and manufactured to precise specifications, including a linear phase characteristic [3].

A sigma-delta A/D Converter consists of an analog block, the "modulator", and a digital block, the "decimator", which consists of a digital filter and a down sampler, as shown in Fig. 1. The modulator is used to sample input signal at oversampling rate which generates an output stream of 1 bit. After over-sampling, it typically performs very coarse analog-to-digital conversion at the resulting narrow-band signal. By using coarse digital-to-analog conversion and feedback, the quantization error introduced by the coarse quantizer is spectrally shaped, i.e., the major portion of the noise power is shifted outside the signal band. This process is called quantization noise shaping. The digital decimation filter removes the out-of-band portion of the quantization error and brings back the output rate to Nyquist rate [4]. Furthermore, in order to simulate any Sigma-Delta A/D converter based system, developers need tested and well-suited models to evaluate the performance of their systems on different development software platform such as MATLAB-SIMULINK and SIMPLORER VHDL-AMS [5]–[6].

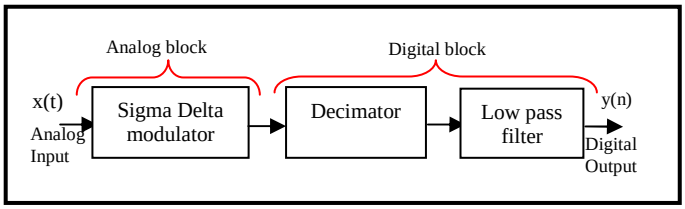

Fig. 1 Diagram of Sigma-Delta ADC

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These performances of sigma-delta modulator like that: Power Spectral Density (PSD), Signal-to-Noise Ratio (SNR), Signal-to-Noise and Distortion Ratio (SNDR) and Effective Number Of Bits (ENOB), … etc., can be affected by a set of non-idealities linked to operational amplifier component, sample and hold operation, thermal noise … etc. Therefore, and in order to enrich the behavioral model libraries of SIMPLORER VHDL-AMS, a behavioral model of second order CIFB sigma-delta modulator is proposed and discussed. The model takes into account most of non idealities such as sampling jitter, kT/C noise and operational amplifier parameters. We also analyze the behavior of the modulator in two case studies: with and without non-idealities model. Finally, simulation results of some parameters as SNR, SNDR and ENOB are presented to evaluate the effects of these non-idealities on the simulation results of PSD.

II. SIGMA-DELTA MODULATOR

A. ADC Description

In the field of high-fidelity audio, high performance Analog-to-Digital Converter (ADC) is greatly needed in computer audio decoder. To keep the audio signal fidelity, the precision of ADC should be as high as 16 bits and the signal bandwidth is in the range which is at least as big as 20 kHz [14],[19]. With traditional ADCs like double-integrating ADC, successive approximation ADC, and folding ADC, it is hard to achieve high precision. So sigma-delta ADC now is more widely used in computer audio decoder chips [21], [12].

A sigma-delta converter consists of an integrator, a comparator and a single bit Digital-to-Analog Converter (DAC, D/A converter), as shown in Fig. 2. The D/A converter is used to make the digital output signal compatible with the analog input signal. The system is based on the oversampling principle, where the input signal sampling frequency is N times higher (oversampling rate) than the Nyquist frequency (two times the higher signal frequency) [27].The output of the DAC is subtracted from the input signal. The resulting signal is then integrated, and the integrator output voltage is converted to a single-bit digital output by the comparator. The resulting bit becomes the input of the DAC and the latter's output is subtracted from the ADC input signal and so on. This closed-loop process is carried out at a very high "oversampled" rate. The digital data coming from the ADC is a stream of "ones" and "zeros," and the value of the signal is proportional to the density of digital "ones" coming from the comparator. This bit-stream data is then digitally filtered and decimated to in a binary-format output [9].

For sigma-delta ADC, there are two traditional structures: single loop structure and multi-stage noise shaping structure (MASH). Each of these structures can be realized with one-bit quantizer or multi-bit quantizer. The single loop sigma delta modulator is not sensitive to mismatch of capacitances and charge leaking. In order to increase the precision high order is needed. Unfortunately, this would make the system conditional stable. MASH modulator is always stable but mismatches of capacitances and charges leaking have big influence on this type of structure. This requires a very good manufacturing process. In addition, MASH modulator has digital part, which would increase the complexity of the circuit [22]. That is why, in this paper, we choose the single loop structure for the evaluation study.

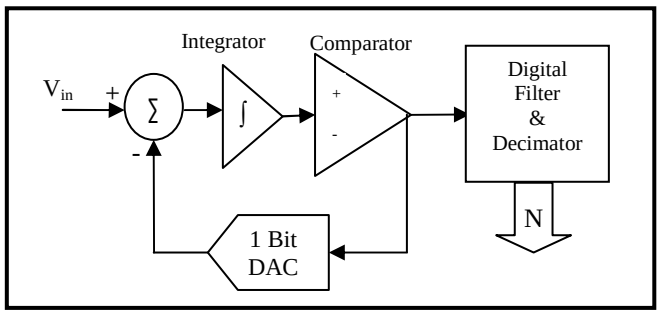

Fig. 2 Sigma-Delta ADC architecture [16]

All sigma–delta feedback topologies may be characterized by two transfer functions: the Noise Transfer Function (NTF) and the Signal Transfer Function (STF). The NTF determines to what extent the quantization noise is reduced in a given bandwidth and hence determines the overall SNDR of the converter. Depending on the chosen architecture, it may or may not be possible to independently specify the STF. From a circuit design point of view, it is desirable to use integrators as the fundamental active building block. This allows the switched-capacitor (SC) circuits to be designed in a parasitic insensitive manner. Meanwhile, by adding a small negative feedback term around pairs of integrators in the loop filter, it is possible to move the open-loop poles, which become NTF zeros when the loop is closed, away from dc along the unit circle [23]. From the consideration mentioned above, a CIFB topology is chosen in this work.

B. CIFB modulator architecture

To describe the behavior of CIFB modulators, we used a powerful development environment: SIMPLORER VHDL-AMS. It is an intuitive, multi-domain, multi-technology simulation program that enables developers to simulate complex power electronic and electrically controlled systems [10]. This high-level hardware description language is an IEEE standard and extension of a digital language VHDL [17]. VHDL-AMS is widely used in electronic design flow for modeling various mixed-signal (analog and digital) circuits and systems including such recent applications as RFID systems [18]-[19]. The bloc diagram of second order CIFB sigma delta modulator implemented with SIMPLORER is given in Fig. 3. Coefficients a_1, a_2 are the feedback gain factors from the quantizer output to the input of the integrator and g is the small feedback term from the output of the second integrator. The chosen coefficient values of the modulator parameters are summarized in Table I. The chosen values are of the same order of magnitude as those available in the most important references [29]-[30].

The Input/Output (I/O) relationship of the designed second-order sigma-delta modulator can be expressed as [25], [26], [28]:

$$Y(z) = STF(z)*X(z) + NTF(z)*E(z)$$

where *STF*(*z*) is the signal transfer function, *NTF*(*z*), the noise transfer function, *E*(*z*), the additive quantization noise, X(z), the modulator input and Y(z) is the modulator output.

For second order CIFB sigma delta modulator presented in Fig. 3, NTF(z) and STF(z) equations are given respectively by:

$$NTF(z) = \frac{(z-1)^2 + g\,c_1}{(z-1)^2 - c_2 a_2 (z-1) + g\,c_1 - c_1 c_2 a_1} \quad (1)$$

$$STF(z) = \frac{c_1 c_2 b_1}{(z-1)^2 + a_2 c_2 (z-1) + g\,c_1 + c_1 c_2 b_1} \quad (2)$$

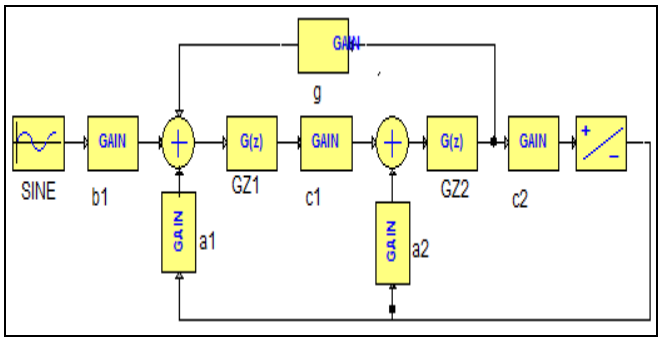

Fig. 3 Second-order CIFB sigma–delta modulator

TABLE I
COEFFICIENT VALUES OF MODULATOR

Coefficient	a_1	a_2	b_1	c_1	c_2	g
Value	0.25	0.25	0.05	0.03	0.4	0.0092

Fig. 4 shows the graphical representation of noise transfer function, NTF, and signal transfer function, STF.

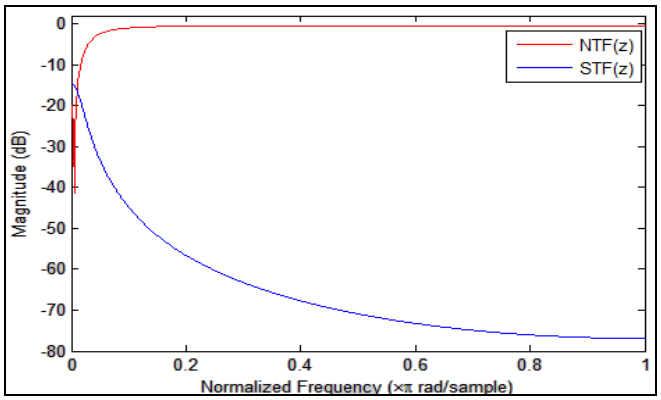

Fig. 4 NTF and STF transfer characteristics

C. Simulation results of second order CIFB modulator

Simulation results are obtained using the "DAY Post Processor" of SIMPLORER. It is a powerful tool to calculate new data channels. This tool includes integration, differentiation, calculation of power characteristics and the Fast Fourier Transform (FFT) of data channels [11]. Parameters values chosen for simulation are summarized in Table II [12], [32], [33].

TABLE II
SIMULATION PARAMETERS

Parameters	Values
Sampling Frequency	Fs = 1 MHz
Amplitude Signal	1 V
Frequency Signal	Fe = 100 kHz
Number of Samples	N = 65536
Integrators $GZ_1(z) = GZ_2(z)$	$\frac{1}{z-1}$

Simulation results are given in Figs 5 and 6. It shows respectively, input and output representations of second order CIFB sigma delta modulator and the Power Spectral Density of the modulator output. We can see that simulation results for ideal CIFB sigma delta modulator are in good agreement with theoretical values.

To characterize the proposed modulator model, we need to evaluate some parameters of the modulator such as SNR, SNDR and ENOB. Simulation results of these parameters are given in Table II. These parameters are defined by:

$$SNR = \frac{P_S}{P_N} \quad (3)$$

$$SNDR = \frac{P_S}{P_N + P_D} \quad (4)$$

$$ENOB = \frac{SNDR - 1.76}{6.02} \text{ [20]} \quad (5)$$

where P_S denotes the signal power, P_N the noise power, and P_D the power of the harmonics of the signal. In an ideal sigma-delta modulator, the SNR is determined only by the quantization noise according to [12]:

$$SNR = \frac{\frac{\Delta^2}{8}}{P_N} = \frac{2^{2N}\,3(2L+1)M^{2L+1}}{2\pi^{2L}} \quad (6)$$

Eq. (6) can be resumed to:

$$SNR = \frac{6(2L+1)M^{2L+1}}{\pi^{2L}} \quad (7)$$

where Δ denotes the input range of the sigma-delta modulator, L is the order of the modulator, M the oversampling ratio ($M = f_s / 2B$, with f denoting the sampling frequency and B the signal bandwidth) and N is the number of bits in the quantizer [13].

Table III, shows simulation results of SNR, SNDR and ENOB values obtained for second order CIFB modulator.

The results obtained are very interesting, however this is an ideal representation of the second order CIFB sigma-delta modulator. Practical implementations will introduce errors which need to be modeled. These errors are common to all sigma delta architectures [8]. The performance of sigma-delta modulator can be affected by a set of non idealities such as sampling jitter, KT/C noise and operational amplifier

parameters (noise, finite gain, finite bandwidth, slew rate and saturation voltages). In the following, we will describe non-idealities models which we implemented in SIMPLORER in a previous work [31].

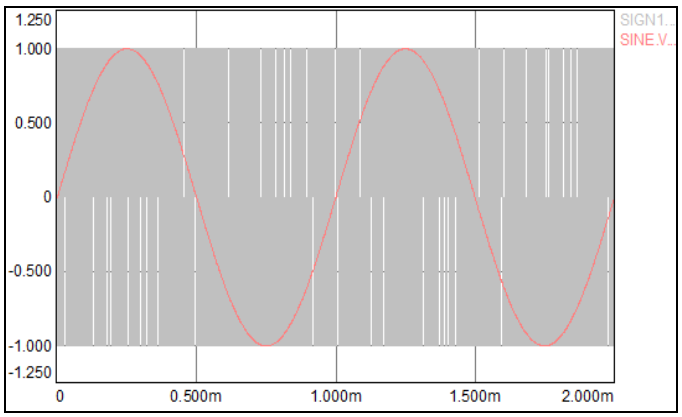

Fig. 5 Input and Output of CIFB modulator

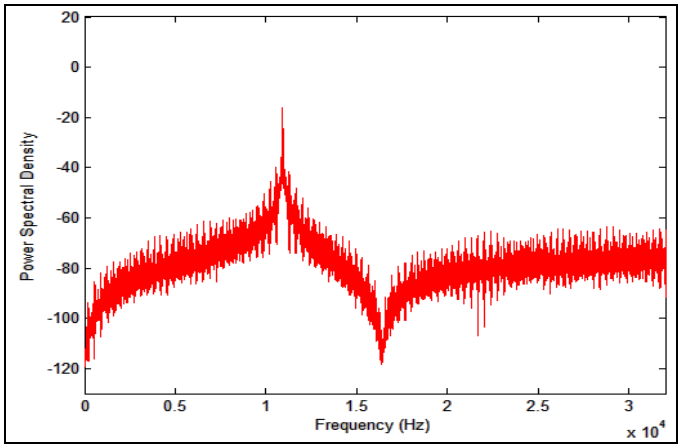

Fig. 6 Power Spectral Density of output modulator

TABLE III
SIMULATION RESULTS OF SECOND ORDER CIFB MODULATOR

Parameter	Value
SNR (dB)	89.55
SNDR (dB)	83.24
ENOB	13.77

III. OVERVIEW OF NON-IDEALITIES MODELS IMPLEMENTED IN SIMPLORER VHDL-AMS

In this section, we will detail models of different errors added to the CIFB sigma-delta modulator: Sampling Jitter, KT/C noise and Op-Amp Noise.

A. Sampling clock Jitter

Sampling clock jitter results in non-uniform sampling and increases the total error power in the quantizer output, as shown in Fig. 7. The magnitude of this error is a function of both the statistical properties of the jitter and the input signal to the converter. The error introduced when a sinusoidal signal with amplitude A and frequency f_{in} is sampled at an instant which is in error by an amount δ is given by [7]:

$$X(t+\delta) - x(t) \approx 2\pi f_{in}\,\delta A \cos(2\pi f_{in} t) = \delta \frac{d}{dt} x(t) \quad (8)$$

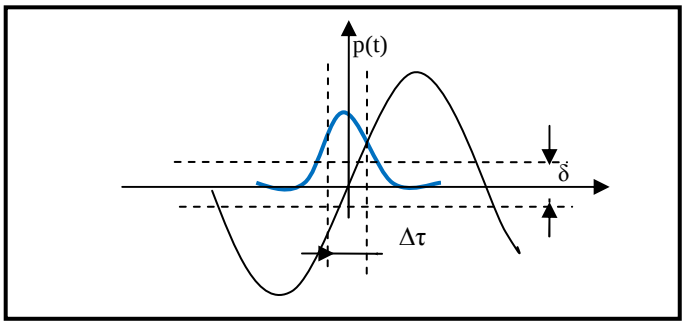

Fig. 7 Effect of clock Jitter in the sampling

This effect can be simulated with SOMPLORER by using the model shown in Fig. 8 which implements Eq. (8). We assumed that the sampling uncertainty δ is a Gaussian random process with standard deviation (parameter 'Gain' in Fig. 8).

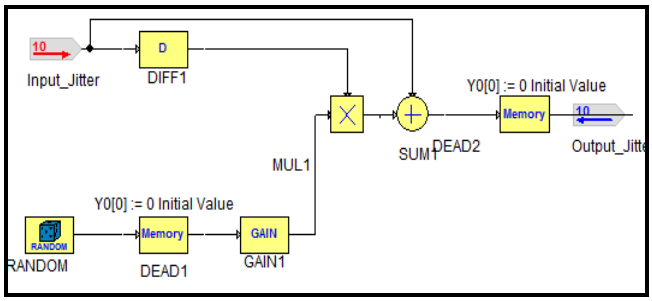

Fig. 8 Modeling of clock jitter with SIMPLORER

B. Op-Amp Noise

In order to realize effective integrators, the use of the operational amplifier (op-amps) is required. However, op-amps can be power hungry devices and much of this power dissipation is related to the gain of the device. It can be shown that loop gain error given by A\(1+A) will shift the modulator poles from their desired locations. This in turn will affect the NTF zeros, moving the signal band noise higher. Fig. 9 shows the model of the op-amp noise implemented in SIMPLORER. The Gain represents the total rms noise voltage referred to the op-amp input.

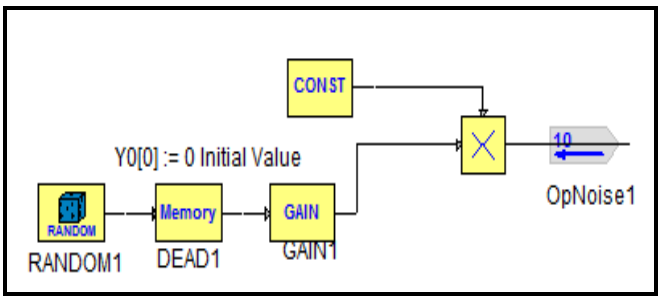

Fig. 9 Modeling of Op-Amp Noise with Simplorer

In this model we considered only thermal noise, while flicker 1\f noise and dc offset are neglected. Indeed, in low-pass Sigma-Delta modulators, flicker noise and dc offset are typically canceled by means of auto-zero, correlated double sampling, or chopper stabilization techniques [13].

C. KT/C Noise

Thermal noise is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium. Thermal noise has a white spectrum and wide band limited only by the time constant of the switched capacitors or the bandwidths of op-amps [10]. Fig. 10 shows behaviour model on SIMPLORER of KT/C noise.

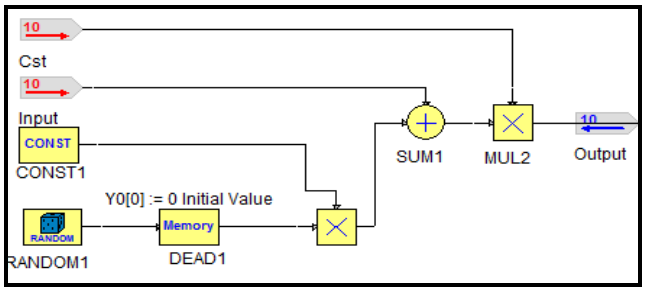

Fig. 10 Modeling of Thermal Noise with Simplorer

Because the KT/C noise is introduced along with the signal at the most beginning, it might be the second most serious noise after the quantization noise and must be taken into consideration. Since the KT/C noise is random in nature, we describe the noise as in Eq. (9) in which α(t) can also be modeled as a Gaussian random process within the range between –1 and 1 [15].

$$e(n) = \sum_C \alpha(t) * \sqrt{\frac{KT}{C}} \qquad (9)$$

IV. ESTIMATION OF EFFECT DUE TO NON-IDEALITIES

Like any analog system, there are inherit of non-idealities [24]. In this section, we will examine the effect of common non-idealities in the context of second order CIFB sigma delta modulator. Fig. 11 shows the block diagram of a second order CIFB structure with non-idealities implemented using the proposed SIMPLORER models.

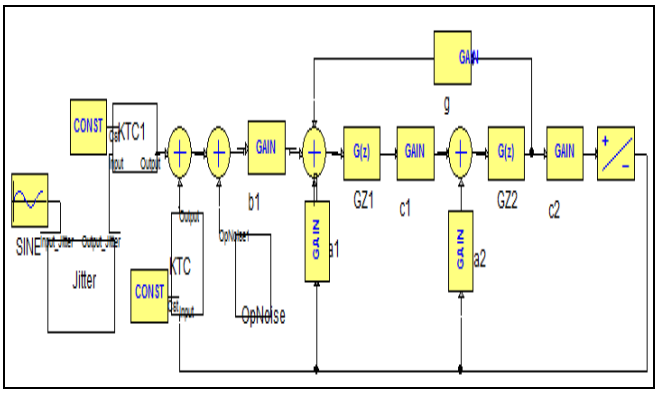

Fig. 11 Block diagram of a second-order CIFB sigma-delta modulator

To validate the models proposed of the various non-idealities affecting the operation of the CIFB sigma-delta modulator, we performed several simulations with VHDL-AMS Simulator where only the non-idealities of the first integrator were considered, since their effects are not attenuated by the noise shaping. The parameters values chosen for the simulation are summarized in Table IV [12], [32], [33]. Simulation results are given in Figs 12 and 13.

TABLE IV
SIMULATION PARAMETERS

Parameters	Value
Signal Amplitude	1 V
Signal Frequency	BW = 100 kHz
Sampling Frequency	Fs = 1 MHz
Number of Samples	N = 65536
Integrating Capacitance of the first integrator	C = 4e-12

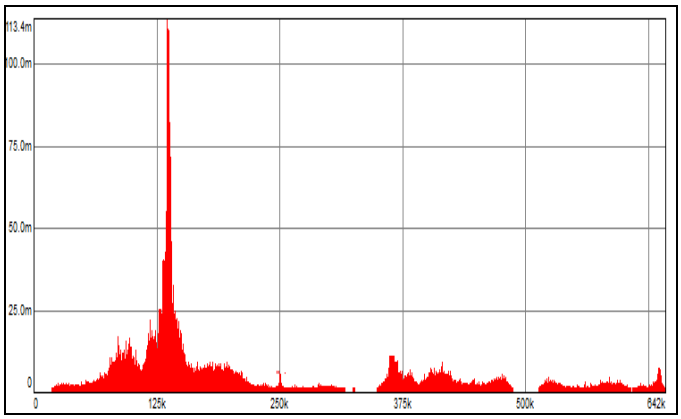

Fig. 12 Spectrum plot of output signal with non-idealities

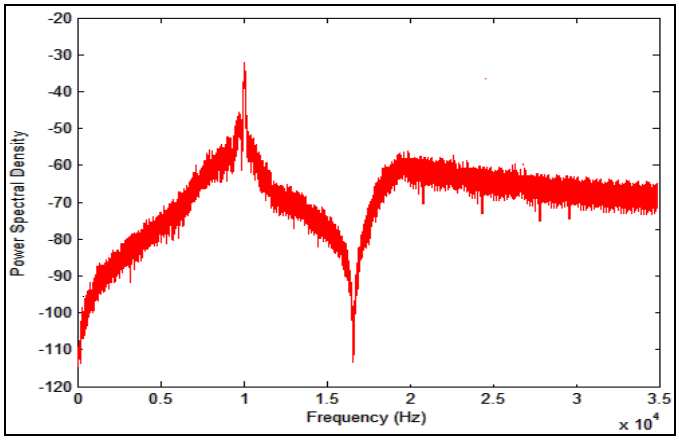

Fig. 13 PSD of second order CIFB Sigma-Delta modulator obtained with SIMPLORER

Fig. 12 shows the frequency response of output signal for non-ideal modulator implemented with SIMPLORER. The magnitude of the second harmonic is about -83 dB, leading to a total harmonic distortion (THD) of about -80 dB, while the signal noise ratio (SNR) is about 89 dB. Fig. 13 presents

power spectral densities (PSD) at the output of the modulator when two of the most significant non-idealities in the first integrator are taken into account. As we can see, there have small errors between two the models of modulator (with and without non-idealities).

It's clear that non-idealities errors affect the performances of the modulator. Harmonics of spectrum plot for non-ideal modulator are more disturbed than the ideal model, so it affects the simulation of signal to noise ratio of the modulator. Also, from results presented in Table V, we note a small difference between simulation results of the two models.

TABLE V
MEASUREMENTS RESULTS OF CIFB MODULATOR WITH NON-IDEALITIES

Parameters	Value
SNR (dB)	88.71
SNDR (dB)	96.40
ENOB	15.77

It is important to note that when an analog signal is sampled, the variation of the sampling period was not a direct effect on circuit performance. Therefore, the clock jitter is only introduced by the sampling signal and thus the effect of this error on a sigma delta converter is independent of the structure of the modulator. Also we can see that, when the jitter error, thermal noise and op-amp errors increase, the spectral density at the output of the quantizer increases.

V. CONCLUSION

In the present work, we presented a complete set of behavior model of second order CIFB Sigma-Delta modulator including the non-idealities of the modulator. We defined three macros implemented with SIMPLORER which describe the behavior of such non-idealities of the modulator: Clock Jitter, Thermal Noise and Operational Amplifier Noise. A simulation result of PSD and frequency response was presented and simulation results of some modulator parameters were analyzed to highlight the model performances. Results obtained are very encouraging for a comparison with actual measurements obtained on a real prototype and also an implementation of these non-idealities on other structures of sigma delta modulators in Simplorer VHDL-AMS.

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