

Newton Raphson algorithm for Selective Harmonic Elimination in Asymmetrical CHB Multilevel Inverter using FPGA

Faouzi ARMI^{#1}, Lazhar MANAI^{*2}, Mongi BESBES^{#3}

[#] Higher institute of information and communication Technologies

B.P N°123 1164- Hammam Chatt- Tunisia

¹armifaouzi@gmail.com

³mongi.besbes@gmail.com

^{*}Research Centre and Energy Technologies

B.P N°95 2050 - Hammam Lif- Tunisia

²manai_lazhar@yahoo.fr

Abstract— Asymmetrical structure is used to reduce the number of bridges and gate drive circuits and DC sources. This structure therefore provides the capability to produce higher voltages at higher speeds with low switching frequency which has inherent low switching losses and high converter efficiency.

Newton Raphson (N-R) algorithm is investigated for the selective harmonic elimination (SHE) to calculate switching angles for a range of variation of the modulation rate 'r' for an asymmetrical cascaded multilevel inverter control.

Based on simulation studies, performance of the proposed algorithm for a nine level asymmetrical cascaded H-bridge inverter, is evaluated and experimentally tested on an prototype using FPGA to implement SHE based on N-R algorithm.

Keywords— Symmetrical/Asymmetrical CHB multilevel inverter, Newton Raphson algorithm, SHE, THD, FPGA.

I. INTRODUCTION

Multilevel inverters are an attractive solutions for the high power applications due to their better performance compared to two-level inverter; there are three types named as diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel [1], [2].

Compared to diode clamped and flying capacitor type, cascaded H-bridge (CHB) inverter requires least number of components to achieve same number of voltage levels and optimized circuit layout is possible because each level have same structure and there is no extra clamping diodes or capacitors [3], [4].

The asymmetrical cascaded multilevel inverters generate a higher number of output levels in comparison with the symmetrical cascaded multilevel inverters with the same number of power electronic devices because of the different amplitude of its DC voltage sources. As a result, the installation space and total cost of an asymmetrical cascaded multilevel inverter is lower than that of a symmetrical cascaded multilevel inverter [5], [6], [7].

Several methods are put forth for the harmonic elimination in literature, such as pulse width modulation (PWM), sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), selective harmonic eliminated pulse width modulation (SHEPWM), all of various switching methods produce harmonics and hence, it is interested in selecting the best method to achieve minimum harmonic and total harmonic distortion [8], [9].

In this study, the lower order harmonics can be eliminated by selection of appropriate switching angle. The various optimization algorithms [10], like partical swarm optimization (PSO) [11], symmetrical polynomial and resultant Theory are used to lower the THD and eliminate the Lower order harmonics. In this paper, the N-R based optimization algorithm is used to eliminate the lower order THD for asymmetrical CHB nine level inverter. The proposed method provides better solution for practical application [12].

FPGAs are digital hardware-based devices and they have become an increasingly popular technology in digital prototyping for multilevel inverters due to their speed and flexibility [13].

In this paper, SHE is suggested for a 9-level asymmetrical H-Bridge inverter. The Newton-Raphson method is used to calculate switching angles with the capability to eliminate the lowest order harmonics (5th, 7th, 11th), while maintaining the fundamental component, in order to generate an optimum stepped output waveform. The analytical results are validated through both simulation and experimental results [14].

This paper is organized as follows. Section 2 describes both power topology of asymmetrical cascaded multilevel inverter and asymmetrical CHB inverter. Harmonic elimination based on N-R optimization is explained in section 3. Simulation and experimental results are presented in section 4 and 5 respectively. Finally, the concluding remarks are drawn in section 6.

II. POWER TOPOLOGY OF ASYMMETRIC AND SYMMETRICAL CHB MULTILEVEL INVERTER

As shown in figure 1, the cascaded multilevel inverter is one of several multilevel configurations. It is formed by connecting single-phase H-bridges inverters in series [15], [3].

In symmetrical cascaded multilevel inverter, where the DC-link voltages of HBs are identical. The number of output levels is normalized by:

$$N = 2h + 1, \quad h: \text{number of H-Bridge} \quad (1)$$

When the number of HB=4, as shown in figure1, therefore the single phase symmetrical inverter output voltage V_{AO} gives a nine level output voltage: $N = 2 \times 4 + 1 = 9$ for $V_{dc1}=V_{dc2}=V_{dc3}=V_{dc4}=E$.

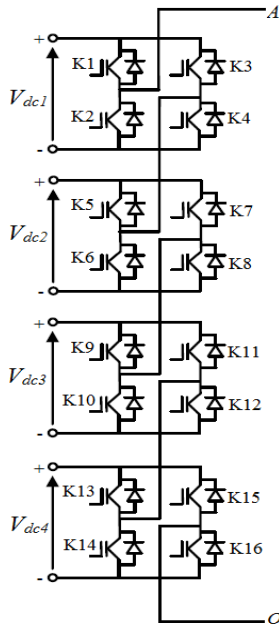


Fig.1 Topology of single phase symmetrical Cascaded 9-level inverter

Unlike symmetrical multilevel CHB inverters which is characterized by partial cells supplied with DC voltages having the same values, asymmetrical converters which are the subject of this study consist of partial cells supplied by different DC voltages, the number of output levels normalized by:

$$N = 2(\sum_{j=1}^h \lambda_j) + 1, \quad \text{where } \lambda_j = \frac{V_{dcj}}{V_{dc1}} \quad (2)$$

Asymmetrical nine levels HB inverter, is obtained for $V_{dc3}=2V_{dc1}=2V_{dc2}=2E$.

$$N = 2(1 + 1 + 2) + 1 = 9.$$

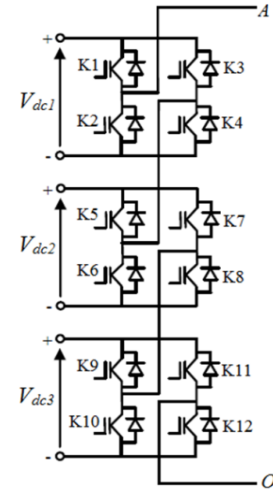


Fig.2 Topology of single phase asymmetrical Cascaded 9-level inverter

The studied asymmetrical 9-level inverter configuration is shown in table 1.

TABLE I
SWITCHING STATES FOR CASCADED SYMMETRICAL 9-LEVEL INVERTER

$V_{dc3}=2V_{dc2}, \quad V_{dc1}=V_{dc2}$				
State	V_{dc1}	V_{dc2}	V_{dc3}	V_{AO}
1	E	E	2E	4E
2	0	E	2E	3E
3	0	0	2E	2E
4	E	0	0	E
5	0	0	0	0
6	-E	0	0	-E
7	0	0	-2E	-2E
8	0	-E	-2E	-3E
9	-E	-E	-2E	-4E

TABLE II
DC-VOLTAGE SOURCES AND SWITCHES COMPARISON
FOR DIFFERENT TOPOLOGIES

Topology	No. of voltage sources	No. of switches	No. of output level
Symmetrical 9-level CHB inverter	4	16	9
Symmetrical 7-level CHB inverter	3	12	7
Asymmetrical 9-level CHB inverter	3	12	9

As shown in table 2, for the same number of bridges, the asymmetrical structure compared to a symmetrical H-bridge topology, can produce a higher number of levels, consequently a better voltage quality, which makes the asymmetrical inverter to be a perfect candidate for selective harmonic elimination.

III. HARMONIC ELIMINATION BASED ON NEWTON RAPHSON ALGORITHM

In this section staircase voltage waveform as shown in figure 3 is chosen for the selective harmonic elimination (SHE) technique in multilevel inverters [16], [6]. The problem under consideration is to find appropriate switching angles namely $\theta_1, \theta_2, \theta_3 \dots \theta_p$ so that the $p-1$ non-triplen odd harmonics can be eliminated and control of the fundamental is also achieved.

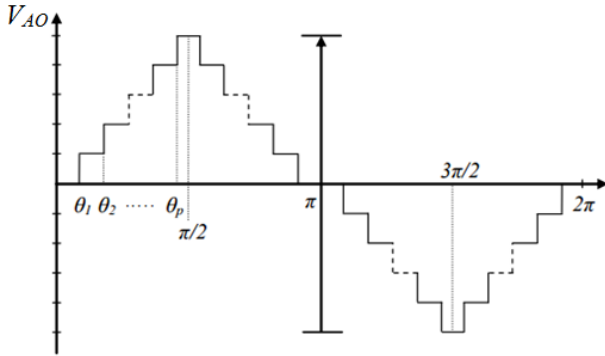


Fig.3 Typical output voltage waveform of a multilevel inverter

Because of the quarter-wave symmetry, the Fourier series expansion of the output voltage V_{AO} , as shown in Figure 3, can be written as:

$$f(\omega t) = \frac{4}{\pi} \int_0^{\pi/2} V_{AO}(\omega t) d\omega t, \text{ for odd } n \quad (3)$$

$$A_n = 0, \text{ for even } n \quad (4)$$

$$B_n = 0, \text{ for all } n \quad (5)$$

$$V_{AO}(\omega t) = \sum_{n=1}^{+\infty} A_n \sin(n\omega t) \quad (6)$$

p and A_n are the number of switching angles and the magnitude of the n^{th} harmonic order respectively, such as:

$$A_n = \frac{4E}{n\pi} \sum_{i=1}^p \cos(n\theta_i) \quad (7)$$

For N -level, in the staircase output voltage waveform, the number of the switching angles p to be calculated is given by:

$$p = \frac{N-1}{2} \quad (8)$$

For a nine level inverter output voltage ($N=9$), the number of harmonics to be eliminated is equal to $(p-1)=3$.

The maximum fundamental voltage is obtained when all the switching angles are zero.

In this case:

$$A_{1max} = \frac{4p}{\pi} V_{dc1} = \frac{16}{\pi} E \quad (9)$$

It is desirable to control the fundamental component of the output voltage at a certain value and eliminate the low-order harmonics as much as possible. In a three-phase and three-wire system the triplen harmonics will be automatically eliminated. In fact, p switching angles are determined by imposing the amplitude of the fundamental component and eliminate the $(p-1)$ harmonics.

In our case, the four switching angles ($\theta_1, \theta_2, \theta_3$ and θ_4) must be determined to eliminate the first three odd harmonic components ($5^{\text{th}}, 7^{\text{th}}$ and 11^{th} order). One solution approach for sets of nonlinear transcendental equations (10) is by applying an iterative method based on Newton Raphson algorithm [17], [18], [19].

$$\begin{cases} \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) = \pi \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) = 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) = 0 \\ \cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) = 0 \end{cases} \quad (10)$$

Modulation rate r is given as follow:

$$r = \frac{A_1}{pV_{dc1}} = \frac{A_1}{pE} : \text{Modulation rate} \quad (11)$$

The Newton_Raphson (N-R) method is one of the fastest iterative methods. Here, the N-R is used in Matlab to solve the set of transcendental equations in (10), and the following matrices are implemented;

The switching angle matrix,

$$\theta^j = \begin{bmatrix} \theta_1^j \\ \theta_2^j \\ \theta_3^j \\ \theta_4^j \end{bmatrix} \quad (12)$$

The nonlinear system matrix,

$$F(\theta) = \begin{bmatrix} \cos(\theta_1) & \cos(\theta_2) & \cos(\theta_3) & \cos(\theta_4) \\ \cos(5\theta_1) & \cos(5\theta_2) & \cos(5\theta_3) & \cos(5\theta_4) \\ \cos(7\theta_1) & \cos(7\theta_2) & \cos(7\theta_3) & \cos(7\theta_4) \\ \cos(11\theta_1) & \cos(11\theta_2) & \cos(11\theta_3) & \cos(11\theta_4) \end{bmatrix} \quad (13)$$

And,

$$\left[\frac{\partial F}{\partial \theta} \right]^j = - \begin{bmatrix} \sin(\theta_1^j) & \sin(\theta_2^j) & \sin(\theta_3^j) & \sin(\theta_4^j) \\ 5\sin(5\theta_1^j) & 5\sin(5\theta_2^j) & 5\sin(5\theta_3^j) & 5\sin(5\theta_4^j) \\ 7\sin(7\theta_1^j) & 7\sin(7\theta_2^j) & 7\sin(7\theta_3^j) & 7\sin(7\theta_4^j) \\ 11\sin(11\theta_1^j) & 11\sin(11\theta_2^j) & 11\sin(11\theta_3^j) & 11\sin(11\theta_4^j) \end{bmatrix} \quad (14)$$

The corresponding harmonic amplitude matrix,

$$T = \begin{bmatrix} r\pi \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (15)$$

Generally, equation (7) can be written:

$$F(\theta) = T \quad (16)$$

By using matrices (11) to (16) and the Newton_Raphson method, the statement of algorithm is shown as follows:

- Guess a set of initial values for θ^j with $j = 0$

Assume,
$$\theta^0 = \begin{bmatrix} \theta_1^0 \\ \theta_2^0 \\ \theta_3^0 \\ \theta_4^0 \end{bmatrix} \quad (17)$$

- Calculate the value of

$$F(\theta^0) = F^0 \quad (18)$$

- Linearize equation (10) about θ^0

$$F^0 + \left[\frac{\partial F}{\partial \theta} \right]^0 d\theta^0 = T \quad (19)$$

And,

$$d\theta^0 = \begin{bmatrix} d\theta_1^0 \\ d\theta_2^0 \\ d\theta_3^0 \\ d\theta_4^0 \end{bmatrix} \quad (20)$$

- Solve $d\theta^0$ from equation (19),

$$d\theta^0 = INV \left[\frac{\partial F}{\partial \theta} \right]^0 (T - F^0) \quad (21)$$

Where $INV \left[\frac{\partial F}{\partial \theta} \right]^0$ is the inverse matrix of $\left[\frac{\partial F}{\partial \theta} \right]^0$

- As updated the initial values,

$$\theta^{j+1} = \theta^j + d\theta^j \quad (22)$$

Repeat the process for equations (15) to (19), until $d\theta^j$ is satisfied to the desired degree of accuracy, and the solutions must satisfy the condition:

$$\theta_1 < \theta_2 < \theta_3 < \theta_4 < \frac{\pi}{2} \quad (23)$$

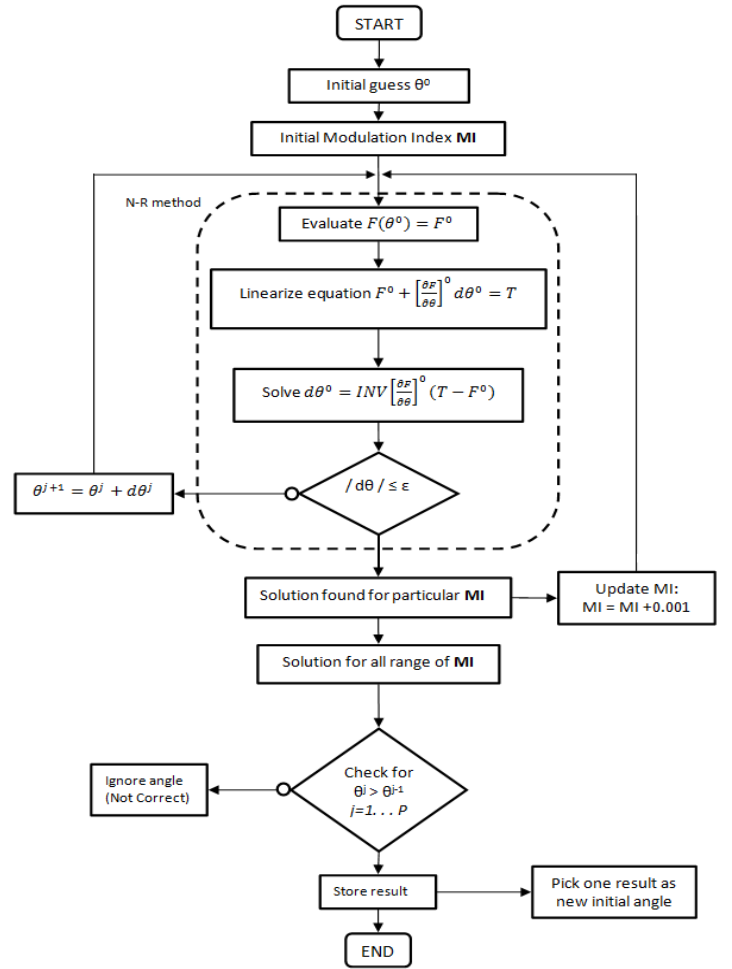


Fig.4 Flowchart of Newton Raphson algorithm

IV. SIMULATION RESULTS

By using MATLAB program, N-R technique returns all the possible combinations of the switching angles for different values of r . The result is represented by figure 5, where one can see the presence of unique solutions of angles for $0.826 \leq r \leq 0.9$ and for $0.925 \leq r \leq 1.0$. On the other side, the system does not accept any solution.

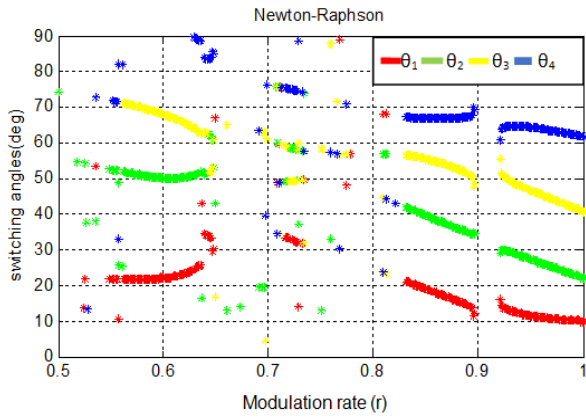


Fig.5 Switching angles versus modulation rate based on N-R algorithm

The residual THD through the 41st harmonic is shown for these solution sets in Figure 6. The THD is defined by:

$$THD(\%) = 100 \times \frac{1}{A_1} \sqrt{\sum_{n=3,5,7...}^{\infty} A_n^2} \quad (24)$$

The best angle values are therefore the ones leading to the lowest THD. The THD is a quantifiable expression for determining how much the signal has been distorted. The greater are the amplitudes of the harmonics, the greater are the distortions.

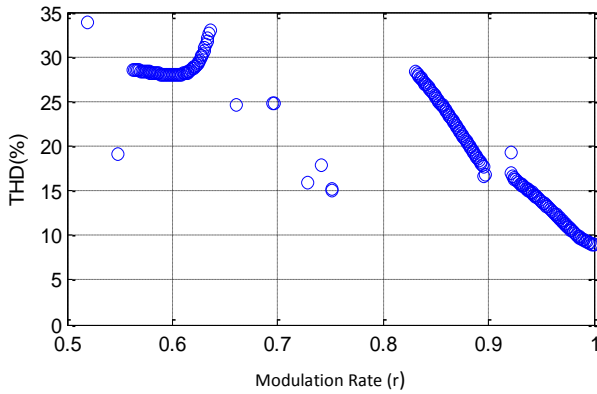


Fig.6 THD vs Modulation Rate based on N-R algorithm

Single phase asymmetrical cascaded nine level inverter is used to drive R-L load ($R = 220\Omega$, $L = 0.5mH$) such as the first HB inverter unit (HB1), second HB inverter unit (HB2) and HB3 DC sources voltages are $V_{dc1} = V_{dc2} = E = 50V$ and $V_{dc3} = 2E = 100V$, respectively. The modulation rate is chosen to be equal to 1, ($r=1$) and output voltage frequency: $f=50$ Hz.

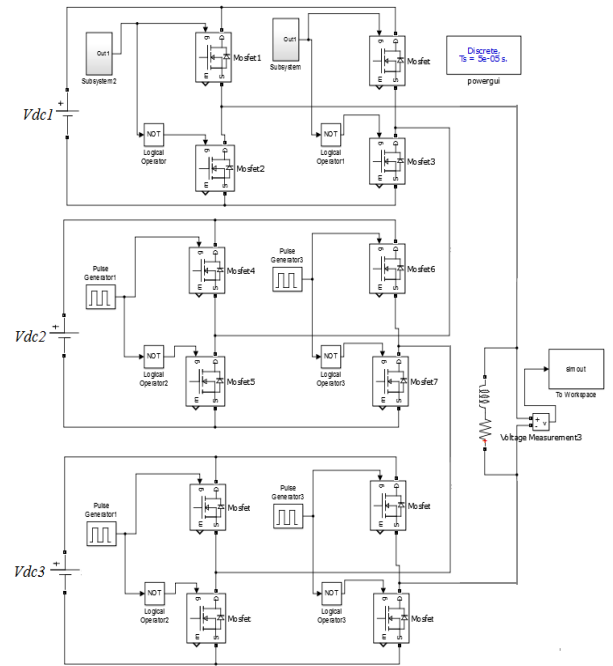


Fig.7 MATLAB/Simulink model of single phase asymmetrical nine level inverter

Using Matlab-Simulink, asymmetrical nine level CHB inverter simulation output voltage and its FFT analysis based equal calculated switching angles (ECSA) technique and N-R algorithm, are depicted in Figures 8, 9, and figures 10 and 11, respectively.

The four switching angles obtained by N-R algorithm such, $\theta_1 = 10.01^\circ$, $\theta_2 = 22.14^\circ$, $\theta_3 = 40.75^\circ$, $\theta_4 = 61.75^\circ$.

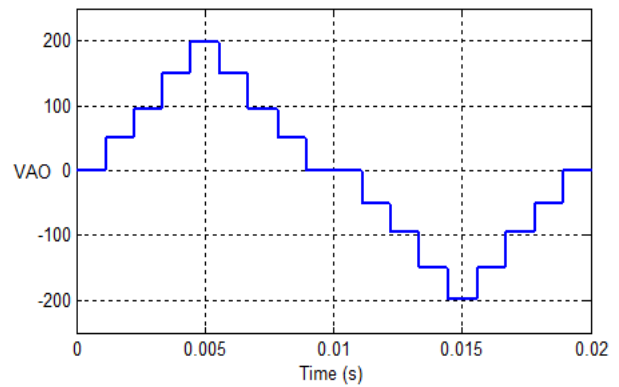


Fig.8 Single phase nine level inverter output voltage waveform (V_{AO}) based on ECSA technique
For, $\theta_1 = \theta_2 = \theta_3 = \theta_4 = 20^\circ$

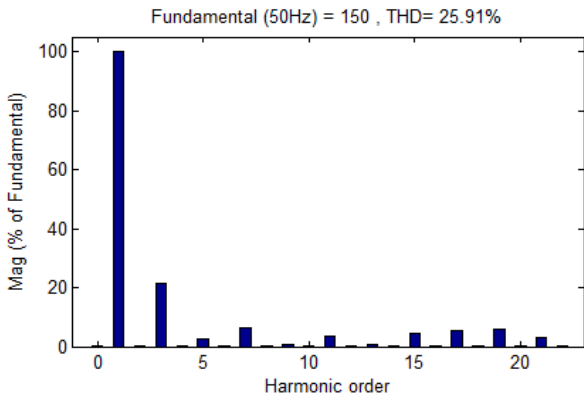


Fig.9 FFT analysis of the nine level inverter output voltage waveform (V_{AO}) based on ECSA

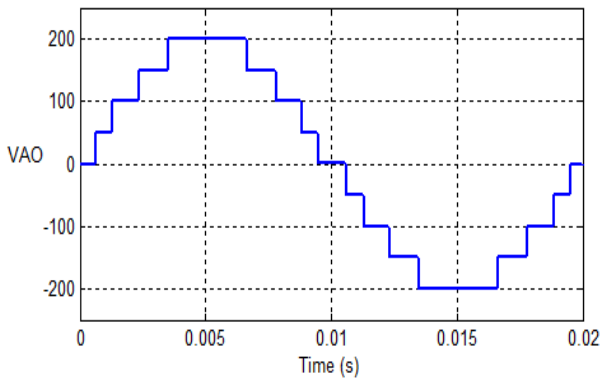


Fig.10 Single phase nine level inverter output voltage wave form (V_{AO}) based on N-R Algorithm
 $\theta_1 = 10.01^\circ$, $\theta_2 = 22.14^\circ$, $\theta_3 = 40.75^\circ$, $\theta_4 = 61.75^\circ$

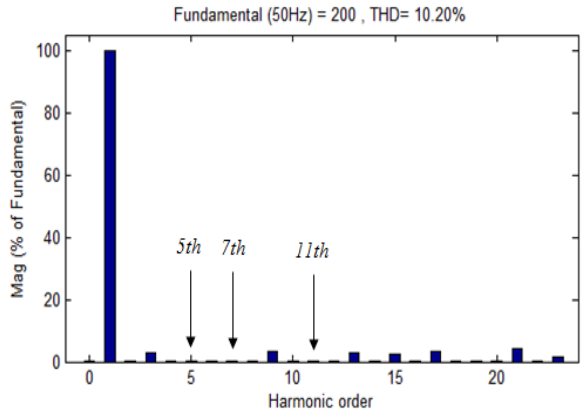


Fig.11 FFT analysis of the nine level output voltage waveform (V_{AO}) based on N-R algorithm for $r=1$

From the spectrum analysis, it is inferred that the THD Newton Raphson based is 10.20% and that for ECSA technique is 25.91%.

In Figure 8 and figure 9 represent the nine level inverter output voltage and its FFT analysis respectively, based on ECSA technique. Figure 9 reveals harmonics 5, 7 and 11 in entirety, reason why the THD is higher than that obtained based on N-R, hence an output voltage waveform represent a poor quality signal. In fact the higher harmonic range in

ECSA technique is explained by the absence of the optimization technique in order to eliminate, 5th, 7th and 11th harmonics. However, figure 11, when N-R algorithm is applied, it is clearly identified that the 5th, 7th and the 11th harmonics are completely eliminated, which explains the significant improvement in harmonic profile.

V. EXPERIMENTAL RESULTS

The SPARTAN 6 VHDL program is verified and simulated using Xilinx-ISE 13.1 software. Once the program is dumped on the FPGA kit, it acts as a controller and generates gating pulses given in figure 7.

The output of the gating signals can be observed in digital storage oscilloscope (DSO) as given in figure 8, where gating signals are generated based on NR algorithm.

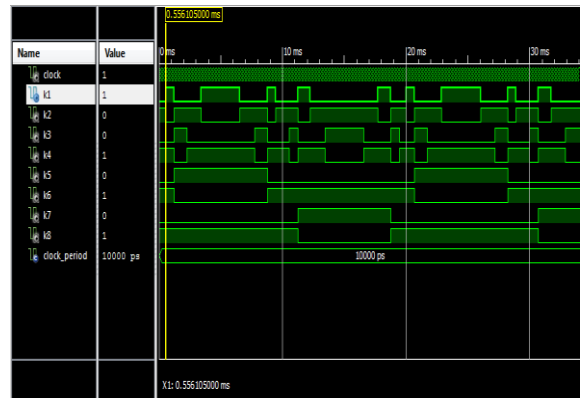


Fig.12 VHDL test bench simulation of the nine levels inverter power switches control signals (K1 - K8)



Fig.13 Photograph of the DSO display the control signals based on NR and generated from FPAG- XILINX

VI. CONCLUSION

This paper has presented a modular method for implementing SHE in an FPGA for a single-phase 9-level asymmetrical CHB multilevel inverter. With the asymmetrical topology, the output quality can be improved with a lower number of switches. Using Newton-Raphson's method, the objectives are achieved by eliminating the 5th, 7th and 11th harmonics of the output voltage.

Simulation results prove the precision and efficiency of the N-R algorithm compared to ECSA.

ACKNOWLEDGMENT

The authors are very much grateful to the officials of the Research Centre and Energy Technologies and Higher institute of information and communication technologies for their financial support and their valuable suggestions.

REFERENCES

- [1] R. Stala, "A natural DC-link voltage balancing of diode-clamped inverters in parallel systems", *IEEE Trans. Ind. Electron.*, Vol. 60, No. 11, pp. 5008-5018, Nov (2013).
- [2] E. Babaei, M. F. Kangarlu, M. Sabahi, and M. R. Alizadeh, "Cascaded multilevel inverter using sub-multilevel cells" *Electr. Power Syst. Res.*, vol. 96, pp. 101–110, (2013).
- [3] A. Kirubakaran, and D. Vijayakumar, "Development of LabVIEW-based multilevel inverter with reduced number of switches", *Int. J. Power Electronics*, Vol. 6, No. 1, pp.88–102, (2014).
- [4] S. Nagaraja, , D.V. Ashok Kumar and C. Sai Babu, "New Multilevel Inverter Topology with reduced number of Switches using Advanced Modulation Strategies", *International Conference on Power, Energy and Control (ICPEC)*, (2013).
- [5] Z. L. Du, M. Tolbert, J.N. Chiasson, and B. Ozpineci, "Reduced Switching-Frequency Active Harmonic Elimination for Multilevel Converters", *IEEE transactions on industrial electronics*, vol. 55, no. 4, (2008).
- [6] K.B. Mohammad, I. E. Hosseinand and B. Frede, "Selective Harmonic Elimination in Asymmetric Cascaded Multilevel Inverters Using a New Low-frequency Strategy for Photovoltaic Applications", *EPCS 43*, (2015).
- [7] E. Babaei, S. Laali, and Z. Bayat, "A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches", *IEEE transactions on industrial electronics*, vol. 62, no. 2, (2015).
- [8] N. Janjamraj, and A. Oonsivilai, "Harmonic Elimination of Hybrid Multilevel Inverters Using Particle Swarm Optimization", *International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering Vol:6, No:12*, (2012).
- [9] V. Nascimento , M. João Viamonte, A. Canito, , N. Silva,"An agent-based electronic market simulator enhanced with ontology matching services and emergent social networks", *Int. J. of Simulation and Process Modelling*, Vol.10, No.3, pp.265 – 278, (2015).
- [10] A. Matías Nacusse, J. Sergio, "Bond-graph-based controller design for the quadruple-tank process", *Int. J. of Simulation and Process Modelling*, 2015 Vol.10, No.2, pp.179 – 191, (2015).
- [11] Z. Huang and H. Zhao "Construction resource scheduling with chaotic particle swarm optimisation", *Int. J. of Simulation and Process Modelling*, 2016 Vol.11, No.1, pp.1, (2016).
- [12] N. Vinoth kumar, V. KumarChinnaiyan and M. Pradish Divekar, "Enhanced power quality of mli using pso based selective harmonic elimination", *International Conference on Green Computing and Internet of Things, ICGCIoT*, (2015).
- [13] W. A. Halim, N. A. Rahim and M. Azri, "Selective Harmonic Elimination for a single-Phase 13-level TCHB Based Cascaded Multilevel Inverter Using FPGA", *Journal of Power Electronics*, Vol. 14, No. 3, pp. 488-498, May 2014.
- [14] Warr, R.L. and Collins, D.H. 'A comprehensive method for solving finite-state semi-Markov processes', *Int. J. Simulation and Process Modelling*, Vol. 10, No. 1, pp.89–99, (2015).
- [15] F. Z. Peng, and J. S. Lai, "Dynamic Performance and Control of a Static Var Generator Using Cascade Multilevel Inverters", *IEEE Transactions on Industry Applications*, Vol. 33, No. 3, (1997).
- [16] L. Karleena, B. Shailaja, M. R. Aravind, and Venkateshappa, "FPGA Implementation of Nine Level Inverter", *International Journal of Engineering Research & Technology (IJERT)*, ISSN: 2278-0181 Vol. 3 Issue 5, (2014).
- [17] B. Diong, H. Sepahvand, and K. A. Corzine, "Harmonic distortion optimization of cascaded H-bridge inverters considering device voltage drops and non integer DC voltage ratios", *IEEE Trans. Ind. Electron.*, Vol. 60, No. 8, pp. 3106-3114, (2013).
- [18] M. K. Bakhshizadeh, H. I. Eini, and F. Blaabjerg, "Selective Harmonic Elimination in Asymmetric Cascaded Multilevel Inverters Using a New Low-frequency Strategy for Photovoltaic Applications", *Electric Power Components and Systems*, 43(8–10):964–96, (2015).
- [19] F. Armi, L. Manai, and M. Besbes, "FPGA implementation of selective harmonic elimination controlled asymmetrical cascaded nine levels inverter using Newton Raphson algorithm", *3rd international conference on automation, control engineering and computer science, ACECS-2016*, paper ID 150.