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Approximation Method for Computing and Reducing Simultaneous Switching Noise in Fast Integrated Circuits

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***Abstract*—In this paper, a study of Simultaneous Switching Noise (SSN) in fast integrated circuit is proposed. First, the problematic of SSN is analysed. Secondly, an analytical method for computing SSN, based on Vector Fitting (VF) approach, is detailed. Then, a technique for reducing this noise is proposed. Finally, the effect of the noise is studied through two different simulators - Pspice and Matlab.**

***Keywords*—Power Distribution Network, Simultaneous Switching Noise, Vector Fitting, Ground-reference planes, Matlab, Pspice.**

I. INTRODUCTION

The embedded system is an electronic system, which includes single microcomputer chip [1]. It configures to perform a specific dedicated application. This system is characterized by its high speed, its lower power dissipation, in addition to its smaller size and high frequency. But one of the problems encountered in these systems is the power integrity, which ensures that all components and transistors have a proper power supply and current that allow them to work in good operating conditions. So, designers should consider all these elements to ensure the power integrity. Beginning at the receiving end of power distribution network (PDN), power is provided out of the IC's power connections by the multi-layer power grid. The power connection congenitally has non-ideals impedance at the latest results in a voltage drop at the transistors [2].

In general, PDN contains many networks of capacitors, inductances and resistors with several types and different values to obtain the impedance target on the frequency range required for ground-reference and power planes of PCB. The design of PDN interconnections should bear its impedance below the target impedance in the high frequency. This will be accomplished by three important principles of design [3, 4]. Although it may not always be possible to push it to the limit, it is always important to be aware of the constraints associated with the actual circuit. As a result, the most important principle to follow, for a profitable design, is to add an appropriate analysis in the design cycle. This will reduce the problems of design and the resulting product will present acceptable performance.

The power supply circuit of the current and voltage source is generally cumbersome and often cannot be directly connected to the transistors presented within the integrated circuits. The currents will therefore have to cross the interconnections of power/reference planes and bonding wires before feeding the transistors. All these elements have a resistance and an inductance and possibly a capacitance. The currents through these elements will therefore create voltage fluctuations at the arrival. Theses fluctuations are called the simultaneous switching noise (SSN). The SSN has many effects near the output of a chip owning to the following reasons [5]. The output drivers switch simultaneously at clock synchronized chips. Then, the outputs drivers, which are very large in size, need a significant amount of instantaneous current to switch and change their states. In addition to the parasitic inductance of the bonding wires in the range of nano-Henries. As a result, it is necessary to reduce the SSN to ensure smooth running of embedded systems.

Different methods have been proposed to reduce SSN, such as adding decoupling capacitors between power and ground-reference planes [6]. There are two primary purposes for using decoupling between power and ground-reference planes. The first purpose is for functionality, that is, the decoupling capacitor is a charge storage device, and when the IC switches state and requires additional current, the local decoupling capacitor supplies this current through a low inductance path. The second purpose for decoupling capacitors is to reduce the noise injected into the power and ground-reference plane pairs and thus reduce the emissions from the edge of the circuit board [7]. Another method to remove noise is the introduction of lossy components serving for the elimination of resonance based on the increase of the component loss [7,8]. Power islands are also used in the reduction of noise by isolating the components making noise on the power bus from sensitive devices [9].

Other technique to reduce noise is used in [28]. In [28], authors propose a novel power-gating structures to reduce noise, more precisely ground bounce, by turning the sleep transistors on in a stepwise manner. This technique serves to

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reduce the fluctuations voltage magnitude, in additions to the required time to stabilize them.

Other method to mitigate SSN is to use the isolation moat, or etched slits, on the power or ground-reference plane [9]. This isolation reduces significantly the radiation level at the frequencies near resonance. Indeed, bridges linking the sides of the etched slits degrade the ability of EMI protection of the etched slits and excite a new low-frequency resonant mode. Selecting the location of the via ports is also a technique to eliminate the noise at higher frequencies [10]. In [10], authors define and develop a novel technique that consists to supress model impedances by reducing transfer and inputs impedances. All these approaches are suitable only to suppress the noise at specific locations. In fact, researches have proposed other manners the reduce the noise in fast integrated circuits. For example, in [11], a novel power/ground plane design have been proposed to eliminate the ground bounce noise (GBN) structure. The proposed structure is efficient given its omni-directionally behaviour. In [12,13], a novel technique to suppress power plane resonance at microwave and radio frequencies has been proposed. The technique concept consists to replace one of the plates of a parallel power plane pair with a high impedance surface or electromagnetic band gap structure. The combination of this technique with a wall of RC pairs extends the lower edge of the effective bandwidth to dc and allows resonant mode suppression up to the upper edge of the band-gap.

Authors in [14] have also given a novel power/ground planes design for efficiently eliminating the ground bounce noise in high-speed digital circuits, this design is based on using low-period coplanar electromagnetic bandgap (LPC-EBG) structure. By Keeping solid for the ground plane and designing an LPC-EBG pattern on the power plane, the proposed structure omnidirectionally behaves highly efficiently in suppression of GBN. The proposed designs suppress electromagnetic interference caused by the GBN within the stopband.

This paper studies simultaneous switching noise (SSN) phenomenon in detail. The main objective of this work is the reduction of SSN. This is achieved firstly by adding the decoupling capacitors to check the paths impedance to ground and power planes. Then by using a proposed technique consisting to isolate the noisy components (digital circuits) of the sensitive components (analogue circuits) by the addition of ground-reference planes with low noise. To analyse and quantify these different phenomena, the PSPICE simulations and the vector fitting method (VFM) are performed.

The paper is organized as follows. Section 2 describes the problematic linking to power distribution network, and the SSN reduction. In section 3, the method of vector fitting is explained and detailed. The results and discussions are included in section 4. Finally, conclusions are drawn in section 5.

II. PROBLEMS OF POWER DISTRIBUTION NETWORK

The aim of the power distribution network design is to provide the sufficient current for each element of the integrated circuit by ensuring that the power supply noise does not exceed the specified margin.

Several papers have discussed the issue of Modeling PDNs. Therefore, there are different modelling methods, such as a finite difference time domain (FDTD) method [30], transmission line method [31, 32], and the transmission matrix method. The transmission line method uses transmission line with two-dimensional array or distributed RLCG elements in SPICE, in addition to the cavity resonator process simulated in SPICE tool [33, 34]. Yet it is essential to mention that the transmission matrix method is based on a modelling cascade of elementary cell circuits RLCG in the package and board [35] which is more effective for analysing PDNs.

The equivalent circuit of a basic power supply network is given by the Figure 1. On this circuit the Vdd voltage between power and ground planes, the load current source and the interconnections are presented. The interconnections are represented by resistances and parasitic inductance Rp, Rg, Lp and Lg respectively. The presence of the current through the supply network impedance induced voltage drops. These variations of the voltages are called the power noise.

The electrical power noise affects the operation of the circuit by several mechanisms. The proper design of the charging circuit ensures a correct operation in accordance with the assumption that the power levels are maintained at an interval close to the levels of nominal voltage. This interval is called the noise margin of the power network.

The main objective in the design of the PDN is to give sufficient current for each transistor of the integrated circuit by ensuring that the power supply noise does not exceed the specified margins. Although, the noise power is a transient phenomenon corresponding to the switching transistors, the design of the PDN is accomplished in the frequency domain. This concept is the method most used by the designers. This method involves the PDN impedance optimization to respect the value of the target impedance. The greatest impedance for the PDN can be obtained by the high impedance that creates a voltage drop always below acceptable ripple specifications [15].

If the PDN impedance remains below the target impedance at each frequency, in the worst case of the supply voltage, the maximum of the transient current through this impedance will be lower than the fluctuations allowed. If the PDN impedance is very less than to the target impedance, this means that the PDN has been badly designed and will be more expensive.

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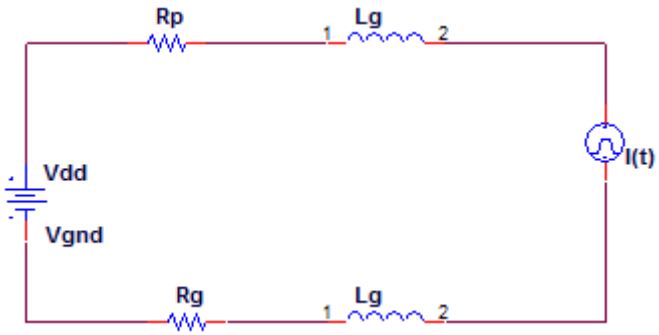

Fig 1. The equivalent circuit of a basic power supply network

A. *Description of Simultaneous Switching Noise*

Simultaneous switching noise (SSN) [16, 17], also referred in the literature as ground bounce, primarily occurs due to very large instantaneous power supply and ground currents propagating within a chip when many transistors are simultaneously switched between on and off states. The magnitude of SSN is found to be proportional to the parasitic inductor L associated with power and ground networks along with the bonding wires that connect pads to pins, and the rate of change of the current through the inductor [18]. SSN noise often leads to serious degradation of signal integrity and overall performance of a chip. It generates glitches on the ground and the power-supply network, it decreases the effective driving strength of the gates, it causes output signal distortion impairing signal integrity, and it reduces the overall noise margin of a system. The effect of SSN is becoming more prominent because of the continuous increase in both chip integration level and system operating speed. Therefore, it is extremely important to accurately model the SSN to ensure high performance and reliable operation of VLSI chips.

The SSN can be calculated by several methods, such as assessing the peak by observing a negative local feedback, in this case it is assumed that internal switching current is small compared to the output driver switching current. However, as the devices are scaled down and the number of gates in a chip increases, the internal switching current becomes comparable to the output driver switching current and can no longer be ignored in the noise calculations [19]. Other method consists to derive an expression for peak value noise and if this peak is a linear function of time during the output transition of the driver [20]. In [20], an analysis of the loading conditions is conducted since no prior knowledge of this is assumed in the design of the package. The sensitivity of SSN to the load capacitance is investigated. The Equations defining a critical capacitance governing SSN are included [20]. Finally, using a vector fitting method to give an approximation of the PDN impedance in the frequency domain is also one of the best method to compute the SSN [21,22,29].

B. *Reduction of noise by adding the ground planes*

Generally, the digital circuits are noisy and share the power in addition to the ground with analogue circuits which are sensitive to noise. If many digital blocks switch simultaneously, the current draw of the distribution network can be significant. This important current pass through the parasitic resistance and inductance of the package, producing voltage fluctuations on the ground-reference planes. Therefore, it results the voltage variations at the analogue circuits sensitive to noise. The figure 2 illustrates the conceptual diagram of two dominant coupling paths of the SSN to an analogue chip on a SIP substrate [23, 24]. The path 1 is the path of the direct coupling propagation of the power supply to the analogue chip through the PDN on-chip and on substrate SiP. The path 2 is the path of coupling SSN to the input signals of the analogue integrated circuit through the transition was in the planes of common references of the substrate SiP. Indeed, by concentrating and basing on the elements of a ground plane, noise reduction can be done as indicated in the introduction.

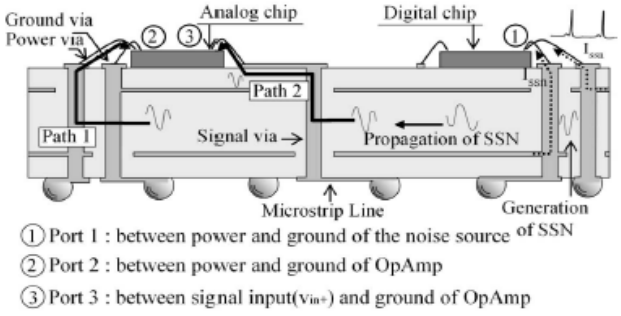

Fig 2. The cross-section view of a SIP circuit describing two paths of the SSN noise of the digital circuit through the package of the substrate SIP to the analogue circuit

III. IMPEDANCE CHARACTERISTIC OF PDN BY VECTOR FITTING

The PDN circuits become more complex, therefore the calculation of its impedance is not obvious. In fact, an approximation in the frequency domain is necessary.

The principle of Vector Fitting consists to give a rational approximation of the impedance or the voltage in the frequency domain as shown in the equation (1).

$$Z_{PDN}(s) \approx d + \sum_{n=1}^{N} \frac{r_n}{s - p_n} \quad (1)$$

Where s is the Laplace variable, p_n is the n-th pole, r_n is the residue corresponding to the n-th pole, N is the order of the rational function, and the term d is real a constant [25,26,27].

The product of the equation (1) with an unknown function $\sigma(s)$; with known poles which we called weighting function; gives the equation (3).

$$\sigma(s) = \sum_{n=1}^{N} \frac{\bar{r}_n}{s - \bar{p}_n} + 1 \quad (2)$$

$$\sum_{n=1}^{N} \frac{r_n}{s - \bar{p}_n} + d \approx \sigma(s).Z_{PDN}(s) \quad (3)$$

Where $\bar{p}_n$ represent the poles of the function $\sigma(s)$ and $\bar{r}_n$ are the residues corresponding to $\bar{p}_n$.

We note that $\sigma(s)$ has the same poles of ($\sigma(s)$. $ZPDN(s)$).

By replacing $\sigma(s)$ by its expression we find:

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$$\sum_{n=1}^{N}\frac{r_n}{s-\bar{p}_n}+d\approx(\sum_{n=1}^{N}\frac{\bar{r}_n}{s-\bar{p}_n}+1).Z_{PDN}(s) \quad (4)$$

$Z_{PDN}(s)$ rational function approximation can be easily obtained from equation (4). So, we find:

$$Z_{PDN}(s)=\frac{(\sigma Z_{PDN})_{fit}(s)}{\sigma_{fit}(s)}=\frac{\prod_{n=1}^{N+1}(s-z_n)}{\prod_{n=1}^{N}(s-\bar{z}_n)} \quad (5)$$

Where:

$$(\sigma Z_{PDN})_{fit}(s)=\frac{\prod_{n=1}^{N+1}(s-z_n)}{\prod_{n=1}^{N}(s-\bar{p}_n)}$$

$$\sigma_{fit}(s)=\frac{\prod_{n=1}^{N}(s-\bar{z}_n)}{\prod_{n=1}^{N}(s-\bar{p}_n)}$$

Equation (5) shows that the poles of $Z_{PDN}(s)$ become the zeros of $\sigma f_{it}(s)$. We observe that the starting poles are cancelled in the process of division because the poles of $(\sigma Z_{PDN}(s))_{\text{fit}}$ are the same of $\sigma f_{it}(s)$. In fact, it is enough to calculate the zeros of $\sigma f_{it}(s)$ to obtain a good set of poles of $Z_{PDN}(s)$ [21,22,26,27,29].

The calculation of the poles and the residues of the impedance rational approximation in the frequency domain can be achieved by the principle of vector fitting in two steps based on the starting poles. The first step involves the identification of the poles based on equation (4) which can be eventually written in this form [27]:

$$\sum_{n=1}^{N}\frac{r_n}{s-\bar{p}_n}+d-(\sum_{n=1}^{N}\frac{\bar{r}_n}{s-\bar{p}_n})Z_{PDN}(s)\approx Z_{PDN}(s) \quad (6)$$

Equation (6) can also be written for k frequency points as a linear problem:

$$[A].\{x\}=\{b\} \quad (7)$$

Where:

$$[A]=\begin{bmatrix} \frac{1}{s_1-\bar{p}_1} & \cdots & \frac{1}{s_1-\bar{p}_N} & 1 & \cdots & -\frac{Z_{PDN}(s_1)}{s_1-\bar{p}_1} & \cdots & -\frac{Z_{PDN}(s_1)}{s_1-\bar{p}_N} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \frac{1}{s_k-\bar{p}_N} & \cdots & \frac{1}{s_k-\bar{p}_N} & 1 & \cdots & -\frac{Z_{PDN}(s_k)}{s_k-\bar{p}_1} & \cdots & -\frac{Z_{PDN}(s_k)}{s_k-\bar{p}_N} \end{bmatrix}$$

$$\{x\}=\begin{bmatrix} r_1 & \cdots & r_N & d & \bar{r}_1 & \cdots & \bar{r}_N \end{bmatrix}^T$$

$$\{b\}=\begin{bmatrix} Z_{PDN}(s_1) & \cdots & Z_{PDN}(s_k) \end{bmatrix}$$

Whit:

k=1,……,N

The vector fitting examined the problem of equation (7) by solving the problem of equation (8) using the least squares method [27], and then passes to the calculation of the zeros by computing the eigenvalues of the matrix H:

$$[H]=[D]-\{c\}\{\bar{r}\}^T \quad (8)$$

Where [D] is a diagonal matrix containing the starting poles, and $\{c\}$ is a column vector of ones, and $\{r\}^T$ is a row-vector containing the residues of $\sigma(s)$.

The second phase of vector fitting consists of calculating the residues of $Z_{PDN}(s)$ directly from equation (5).

The rational approximation with the vector fitting in frequency domain should respect several criteria such as passivity, causality and stability. The passivity is satisfied when the eigenvalues of $\text{Re}\{Z_{PDN}(s)\}$ are strictly positive [36]. This leads to the optimization stage:

$$\Delta Z_{PDN}(s)=\sum_{n=1}^{N}\Delta\frac{r_n}{s-p_n}+\Delta d\cong 0 \quad (9)$$

$$eig(\text{Re}\{Z_{PDN}(s)+\Delta d+\sum_{n=1}^{N}\frac{\Delta r_n}{s-p_n}\})>0 \quad (10)$$

The first part of equation (9) minimizes the variation in the impedance matrix elements, whereas the second imposes the criterion of passivity on the disturbed model [37]. The stability can be satisfied by controlling the rational approximation poles. The stability condition is, thus, equivalent to granting that the poles lie in the left-hand plane. Finally, the causality is satisfied when we reach $\text{Re}(p_n)<0$ [38].

After having respected these three criteria, $Z_{PDN}(s)$ can be written in the frequency domain as:

$$Z_{PDN}(s)=d+\sum_{m=1}^{M}\frac{a_m}{s-b_m}+\sum_{n=1}^{N}\frac{2r_{nr}(s-p_{nr})-2r_{ni}p_{ni}}{(s-p_{nr})^2+p_{ni}^2} \quad (11)$$

Where the N poles p_{nr}-jp_{ni}, p_{nr}+jp_{ni} and their corresponding residues r_{nr}- jr_{ni}, r_{nr}+jr_{ni} are complex conjugate pairs, and the M poles b_m and its corresponding residues a_m are real.

By performing the inverse Laplace transformation, the impedance in the time domain has the following form:

$$z_{PDN}(t)=d\,\delta(t)+\sum_{m=1}^{M}a_m e^{b_m t}\,h(t)+2\sqrt{(r_{nr}^2+r_{ni}^2)}\,e^{p_{nr}t}\cos(p_{ni}t+\varphi)\,h(t) \quad (12)$$

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Where: $\delta(t)$ is the Dirac impulsion and $h(t)$ is the unit step function and:

$$\varphi = ar\cos\frac{r_{nr}}{\sqrt{r_{nr}^2 + r_{ni}^2}}$$

It is clear that the impedance function in the time domain can be easily obtained from the rational approximation in the frequency domain.

Once the impedance function in the time domain is determined from equation (2), the SSN waveform can be calculated as follows:

$$v_{noise}(t) = [d\,\delta(t) + \sum_{m=1}^{M} a_m e^{b_m t}\,h(t) + 2\sum_{n=1}^{N}\sqrt{(r_{nr}^2 + r_{ni}^2)}\,e^{p_{nr}t}\cos(p_{ni}t + \varphi)\,h(t)] * i_{load}(t) \quad (13)$$

Where * denotes the convolution operation.

IV. Results and Discussion

To study the effectiveness of the noise reduction on the ground-reference plane, a simplified model of the technique is used, as shown in Figure 3. The noise associated with the ground, induced by the simultaneous switching in the digital circuit, is modelled by a voltage source. The voltage source used is sinusoidal with amplitude of 100mV at a given frequency. The interconnections are modelled by R_p and L_p and the decoupling capacitor by R_d, L_d and C_d. The noise reduction technique between the noisy source and the receiver circuit (sensitive to noise) is based on the impedance of the ground path between the terminals (noisy circuit and sensitive circuit). This impedance is modelled by a RL circuit which is presented by R_{c1} and L_{c1} as shown in the figure 3. These elements are given by unit of length.

The maximum voltage on the ground victim is evaluated using PSPICE and VFM based on the distance (x) between the digital and analogue circuits. The simulations are performed for x ranging from 1 to 10 (unit of length).

The ground noise reduction view by the circuit victim (analogue circuit VQ_{gnd} is represented as a function of the separation x as shown in the figure 4.

According to the Figure 4 we note that the noise reduction is about 52% which is reached for ten-unit lengths between the digital and analogue blocks. The figure shows that when x increases, the noise decreases. Improved results can be achieved if the ground-reference plane impedance is smaller than the impedance between the sensitive circuits to noise and the noisy circuits.

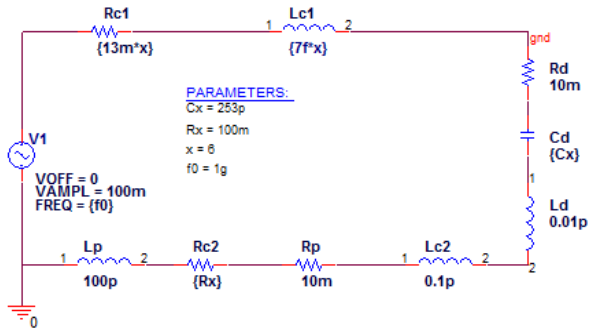

Fig. 3. The equivalent circuit of the noise reduction technique (ground plane)

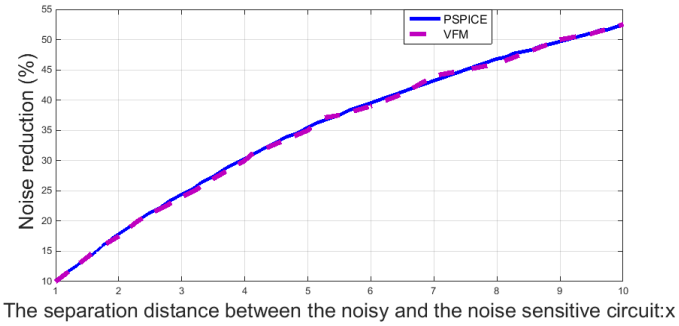

Fig. 4. The reduction of noise versus the separation distance between the circuit aggressors and the circuit victims

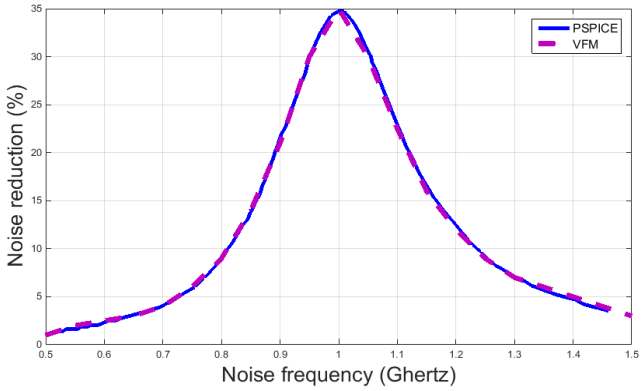

Fig. 5. The noise reduction for a sinusoidal noise source according to the frequency

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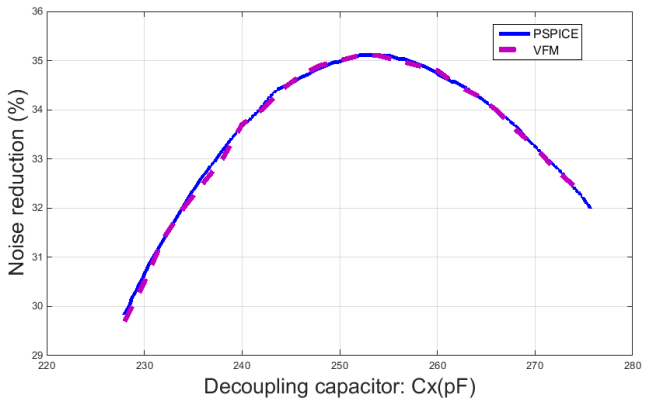

Fig. 6. The noise reduction for a sinusoidal noise source according to the decoupling capacitors

The variations effects of the frequency f_0 of the noise signal as well as the decoupling capacitors C_d are simulated by the PSPICE tool and compared by VFM. It is considered that f_0 varies from 50% of the resonance frequency of the RLC circuit, and that C_d varies from 10% of the target value 253pF. These values are chosen for a typical CMOS technology. The effectiveness of the reduction of the ground noise for a sinusoidal noise source for several values of frequency and decoupling capacitors is illustrated respectively in figures 5 and 6.

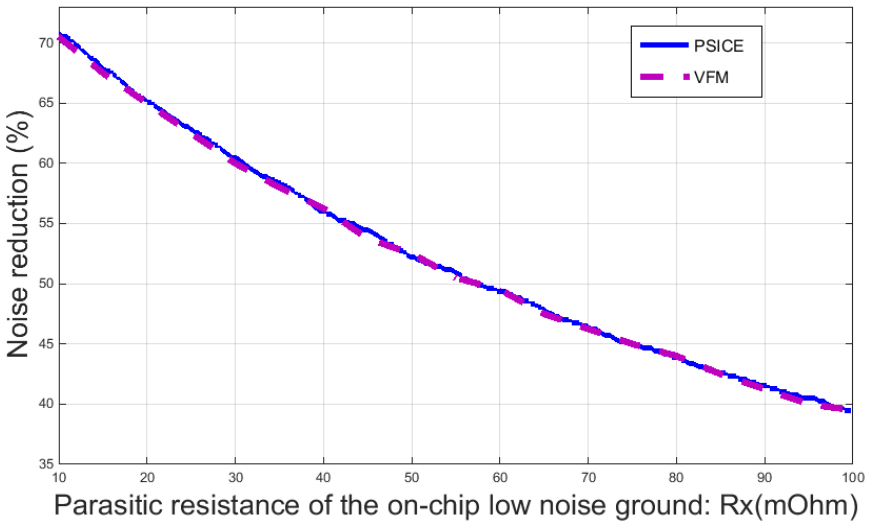

Fig. 7. The noise reduction for different values of the parasitic resistance of the ground plane

Since the equivalent inductance of the ground plane between digital and analog circuits is not compensated, the noise surrounding f_0 is not much reduced.

As indicated in figure 6, the ground noise is weakly dependent of the decoupling capacitor C_d. In this technique the noise is reduced by 4% over the range of C_d value.

The impedance of the ground plane added is purely resistive at the resonance frequency. The ground noise reduction and the ground-reference noise view of the circuit victim for several values of R_x are given by the figure 7.

The curves of the figure 7 show that the reduction of the noise may reach 70% for low values of R_x.

V. Conclusions

The establishment of a stable network power supply requires that the power planes impedance is lower than the target impedance. As an effect, it is necessary that the variation of the voltage does not exceed a specific level.

The interaction between the signal integrity and the power supplies integrity, also called the simultaneous switching noise (SSN), has been examined in detail on the complex and fast chip. The simultaneous switching will induce a significant voltage drop in the power. These simultaneous switching generates instability of the power planes and degrades the levels of the outputs of the transistors. The noise reduction technique proposed is to add a ground-reference planes between the digital circuit aggressor and the analog circuits sensitive to noise. The results obtained show the effectiveness of the technique used which helps to reduce the SSN and show also the coincidence of the two curves given by PSPICE and VFM.

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